

Veyron-R

CPU : Sandy Bridge PGA
Chip Set : Intel Cougar Point
GFX : N12P-GS
Remarks : Huron River Platform

Model Name : Veyron-R
PBA Name : MAIN
PCB Code : BA41-01471A (GCE)
BA41-01472A (GBM)
BA41-01473A (NY)

Dev. Step :
Revision : 1.0
T.R. Date : 2011.06.24

Design	CHECK	APPROVAL
<i>GU HUI</i>	<i>SJ WU</i>	<i>BC LEE</i>

■ Owner : SRDC PD3

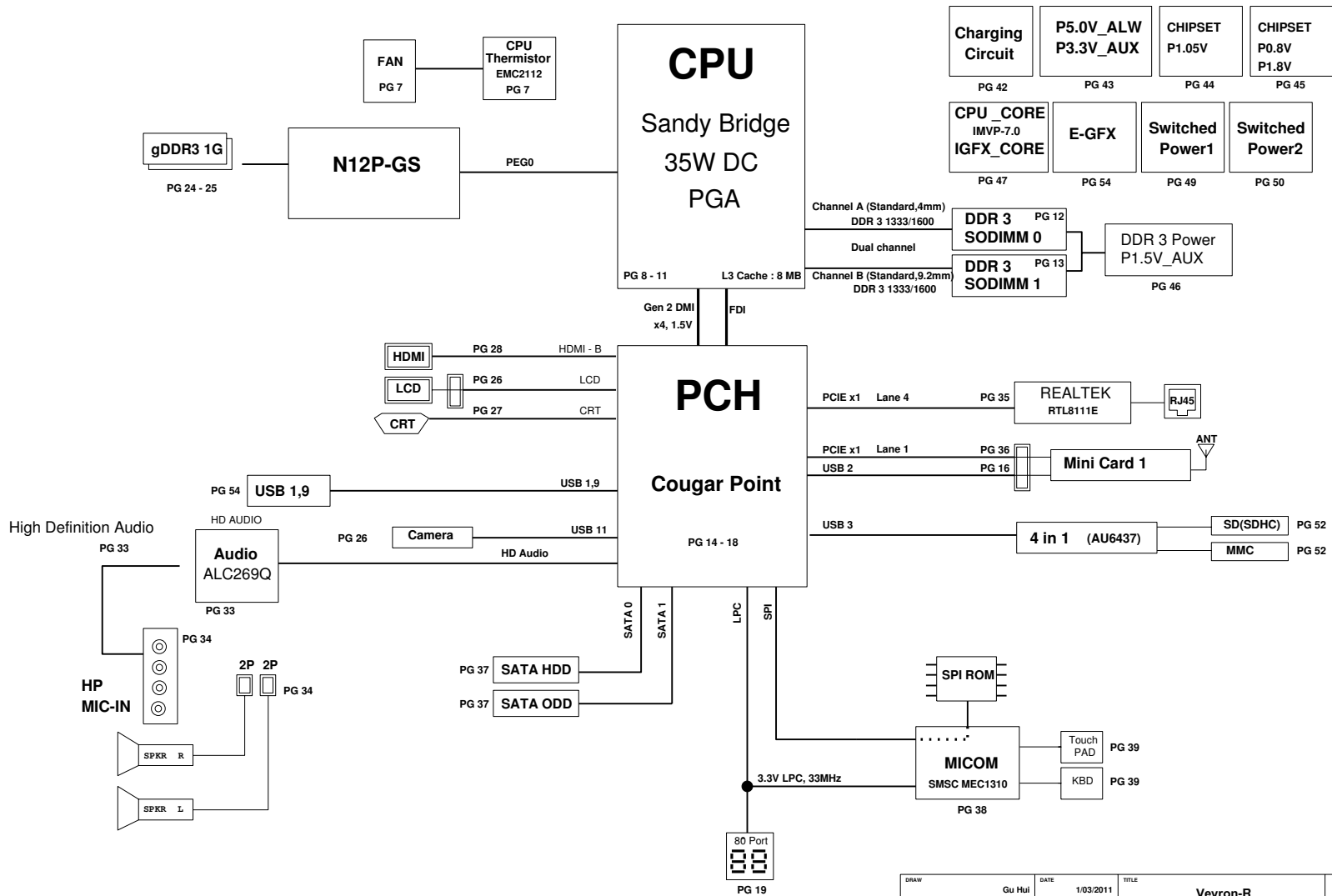
Signature : *GUHUI*

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DRAW	Gu Hui	DATE	1/03/2011	Veyron-R MAIN COVER	SAMSUNG ELECTRONICS
CHECK	SJ Wu	DEV. STEP	ADV		
APPROVAL	BC LEE	REV	rev. 0.1		
MODULE CODE	LAST EDIT				
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BLOCK DIAGRAM



DRAW	Gu Hui	DATE	1/03/2011	TITLE	Veyron-R	SAMSUNG
CHECK	SJ Wu	DEV. STEP	ADV		MAIN	ELECTRONICS
APPROVAL	BC LEE	REV	rev. 0.1		BLOCK DIAGRAM	PART NO. BA41-01XXXA
MODULE CODE	undefined	LAST EDIT	January 20, 2011 18:58:20 PM	PAGE	2	OF 48

BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails	Active in
VDC P3.3V_MICOM P5.0V_STB P5.0V_ALW P3.3V_ALW P12.0V_ALW	Primary DC system power supply (7 to 21V) 3.3V always power rail (for Micom) 5.0V always power rail 5.0V always power rail 3.3V always power rail 12.0V always power rail
P5.0V_AUX P3.3V_AUX P1.5V_AUX	5.0V switched on power rail (off in S4-S5) 3.3V switched on power rail (off in S4-S5) 1.5V power rail for DDR3 (off in S4-S5)
P5.0V P3.3V P1.8V P1.5V P0.75V P0.8V	5.0V switched power rail (off in S3-S5) 3.3V switched power rail (off in S3-S5) 1.8V switched power rail (off in S3-S5) 1.5V switched power rail (off in S3-S5) 0.75V power rail for DDR3 (off in S3-S5) 0.8V switched power rail (off in S3-S5)
VCC_CORE EGFX_CORE P1.05V (VCCP)	Core Voltage for CPU Core Voltage for GPU VCC for COUGARPOINT
P3.3V_D P1.5V_D P1.05V_D	3.3V descrete power rail for N12X 1.5V descrete power rail for N12X 1.05V descrete power rail for N12X

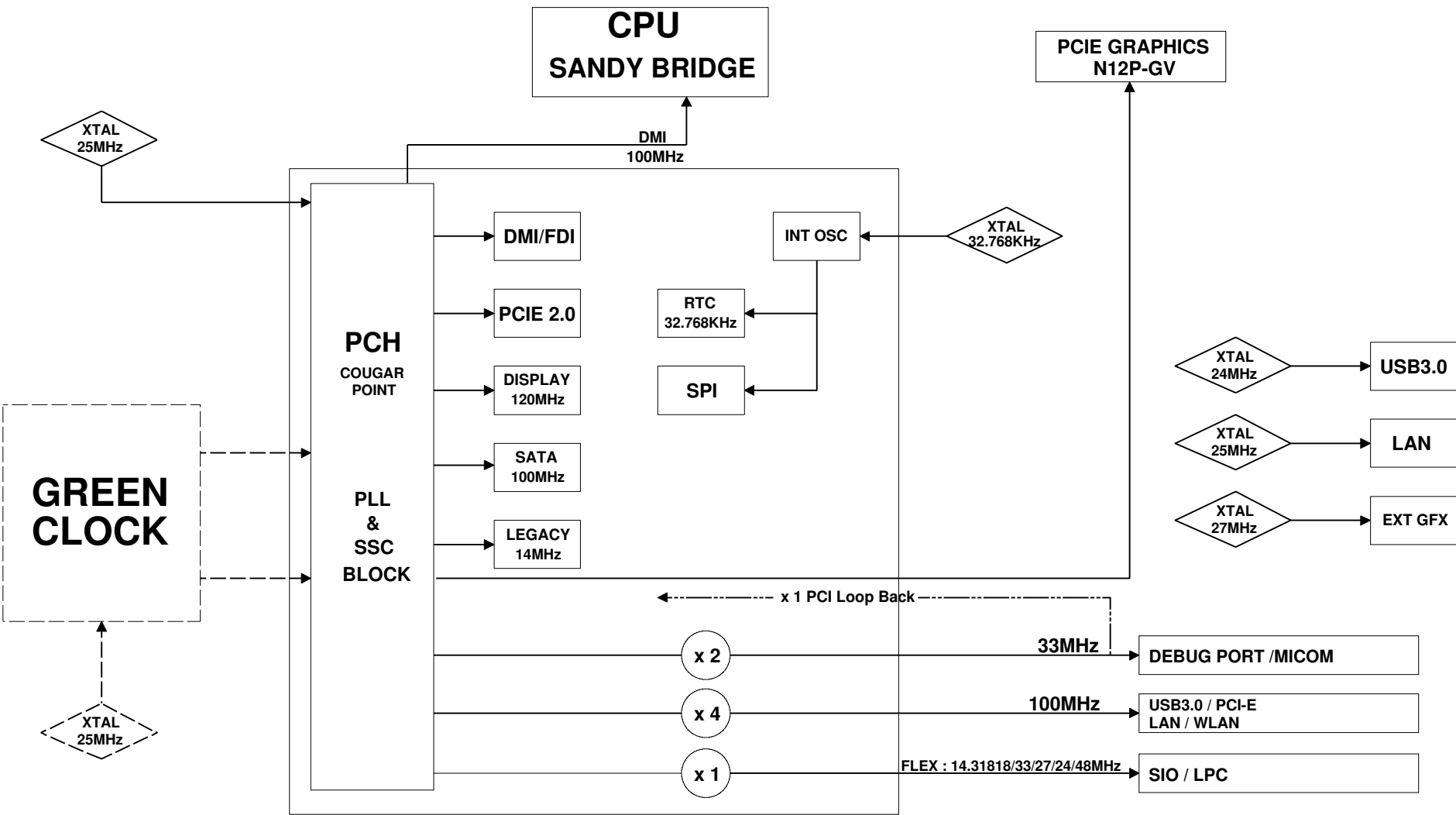
USB PORT Assign	PCI Express Assign
PORT # ASSIGNED TO	PORT # ASSIGNED TO
0 NC	1 Mini Card 1 (WLAN)
1 SYSTEM PORT 0	2 NC
2 Mini PCI Express	3 NC
3 Multi Memory Card Controller	4 LAN CONTROLLER
4 NC	5 USB 3.0
5 NC	6 NC
6 NC (N/A WITH HM55)	7 NC
7 NC (N/A WITH HM55)	8 NC
8 Camera	
9 SYSTEM PORT 1	
10 NC	
11 Camera(LCD Cable)	
12 NC	
13 NC	

SATA PORT Assign
PORT # ASSIGNED TO
0 HDD
1 ODD
2 (N/A WITH HM65)
3 (N/A WITH HM65)
4
5

Crystal / Oscillator			
TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	HM65	Real Time Clock
Crystal	25MHz	LAN	Intel LAN
Crystal	24MHz	USB 3.0	
Crystal	25MHz	HM65	INTEL
Crystal	27MHz	N12P-LP	NVIDIA

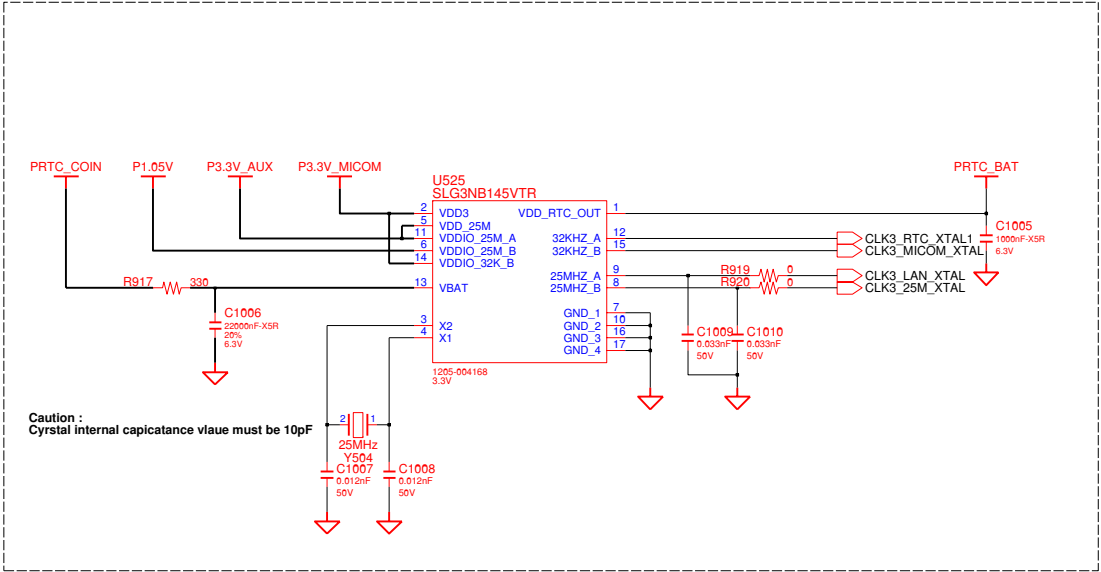
LCD Pannel Detect (TBD)		
Devices	Resolution	PANNEL_DETECT_0

I ² C / SMB Address			
Devices	Address	Hex	Bus
HM65	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	-
SODIMM0	1010 000x	A0h	Thermal Sensor
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
Thermal Sensor on board	1101 100x	98h	
Power thermal management TS	1101 011x	96h	



DRAW	Gu Hui	DATE	1/03/2011	TITLE	Veyron-R	SAMSUNG
CHECK	SJ Wu	DEV. STEP	ADV	MAIN	MAIN	ELECTRONICS
APPROVAL	BC LEE	REV	rev. 0.1	CLOCK DIAGRAM	PART NO.	BA41-01XXXXA
MODULE CODE	undefined	LAST EDIT	January 20, 2011 18:58:20 PM	PAGE	5	OF 48

CLOCK DISTIBUTOR



GREENCLK
GREENCLK
GREENCLK
GREENCLK
GREENCLK
GREENCLK
GREENCLK
GREENCLK
GREENCLK
GREENCLK

D

0	0101 111xb
✓ HIGH Z	0111 101xb (7A)
1	0101 110xb

0	INTEL TR MODE
HIGH Z	AMD CPU/DIODE MODE
✓ 1	EXT.DIODE 2 MODE

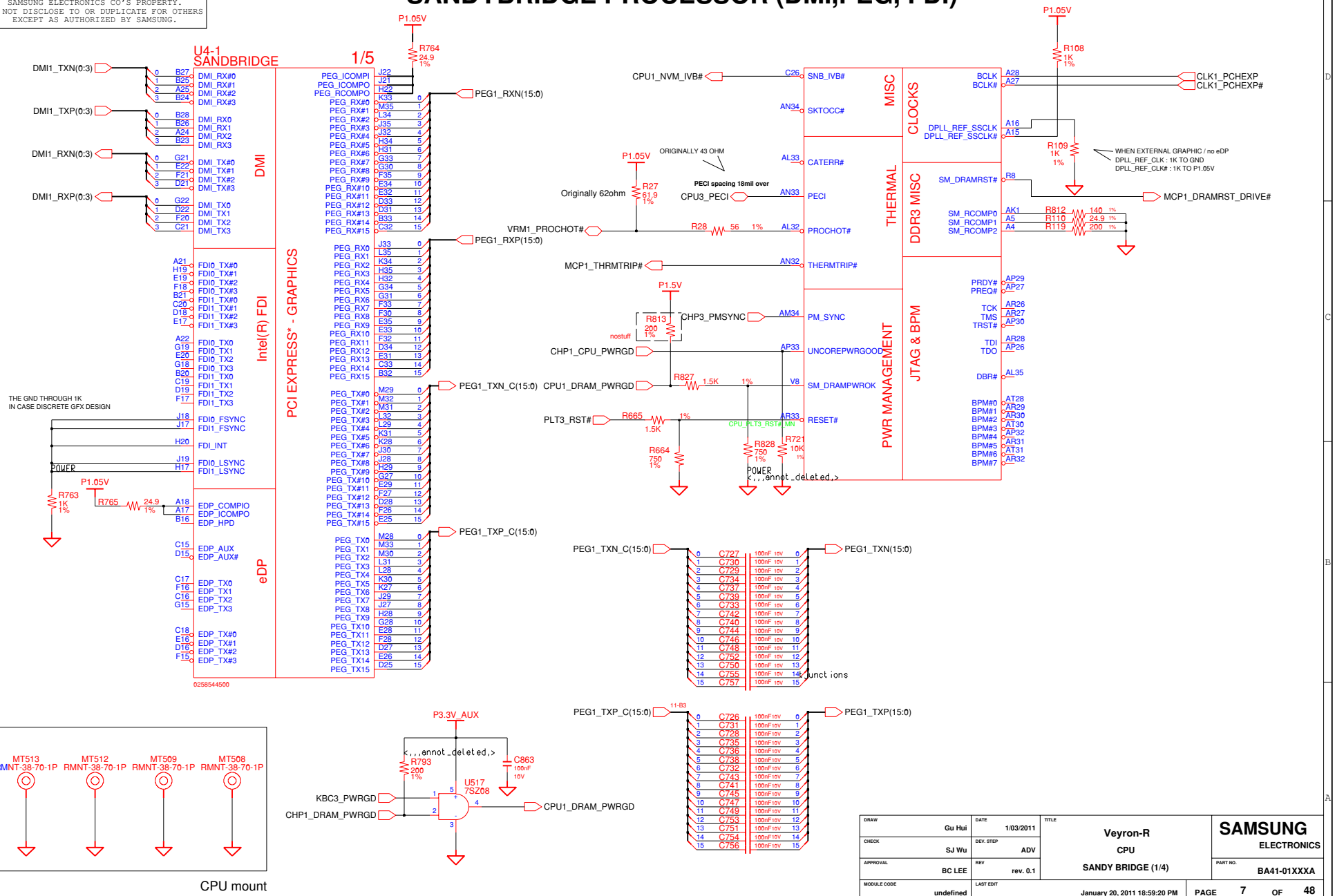


B



2

SANDYBRIDGE PROCESSOR (DMI,PEG, FDI)

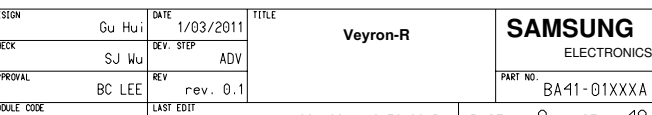


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CHECK	SJ Wu	DEV. STEP	ADV			PART NO. BA41-01XXXX
APPROVAL	BC LEE	REV	rev. 0.1		SANDYBRIDGE (1/4)	
MODULE CODE	undefined	LAST EDIT				

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DRAW	Gu Hui	DATE	1/03/2011	Veyron-R CPU SANDY BRIDGE (2/4)	SAMSUNG ELECTRONICS
CHECK	SJ Wu	DEV. STEP	ADV		
APPROVAL	BC LEE	REV	rev. 0.1		
MODULE CODE	undefined	LAST EDIT	January 20, 2011 18:59:20 PM		
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**U4-5
SANDBRIDGE 5/5**

AT35	VSS1	VSS81	AJ22
AT32	VSS2	VSS82	AJ19
AT29	VSS3	VSS83	AJ18
AT27	VSS4	VSS84	AJ13
AT25	VSS5	VSS85	AJ10
AT22	VSS6	VSS86	AJ7
AT19	VSS7	VSS87	AJ4
AT16	VSS8	VSS88	AJ3
AT13	VSS9	VSS89	AJ2
AT10	VSS10	VSS90	AH35
AT7	VSS11	VSS91	AH34
AT4	VSS12	VSS92	AH33
AT3	VSS13	VSS93	AH32
AP26	VSS14	VSS94	AH30
AP22	VSS15	VSS95	AH29
AP19	VSS16	VSS96	AH28
AP16	VSS17	VSS97	AH26
AP13	VSS18	VSS98	AH25
AP10	VSS19	VSS99	AH22
AP7	VSS20	VSS100	AH19
AP4	VSS21	VSS101	AH16
AP2	VSS22	VSS102	AH7
AP31	VSS23	VSS103	AH3
AP28	VSS24	VSS104	AG9
AP25	VSS25	VSS105	AG8
AP22	VSS26	VSS106	AG4
AP19	VSS27	VSS107	AF5
AP16	VSS28	VSS108	AF3
AP13	VSS29	VSS109	AF2
AP10	VSS30	VSS110	AF2
AP7	VSS31	VSS111	AE35
AP4	VSS32	VSS112	AE34
AP1	VSS33	VSS113	AE33
AN30	VSS34	VSS114	AE32
AN27	VSS35	VSS115	AE30
AN25	VSS36	VSS116	AE29
AN22	VSS37	VSS117	AE28
AN19	VSS38	VSS118	AE27
AN16	VSS39	VSS119	AE26
AN13	VSS40	VSS120	AE2
AN10	VSS41	VSS121	AD7
AN7	VSS42	VSS122	AD7
AN4	VSS43	VSS123	AC9
AM29	VSS44	VSS124	AC8
AM26	VSS45	VSS125	AC6
AM22	VSS46	VSS126	AC3
AM19	VSS47	VSS127	AC2
AM16	VSS48	VSS128	AC2
AM13	VSS49	VSS129	AB35
AM10	VSS50	VSS130	AB34
AM7	VSS51	VSS131	AB32
AM4	VSS52	VSS132	AB31
AM3	VSS53	VSS133	AB30
AM2	VSS54	VSS134	AB29
AM1	VSS55	VSS135	AB28
AL34	VSS56	VSS136	AB27
AL31	VSS57	VSS137	AB26
AL28	VSS58	VSS138	AB26
AL25	VSS59	VSS139	Y8
AL22	VSS60	VSS140	Y6
AL19	VSS61	VSS141	Y5
AL16	VSS62	VSS142	Y4
AL13	VSS63	VSS143	Y2
AL10	VSS64	VSS144	W35
AL7	VSS65	VSS145	W34
AL4	VSS66	VSS146	W33
AL2	VSS67	VSS147	W31
AK33	VSS68	VSS148	W31
AK30	VSS69	VSS149	W30
AK27	VSS70	VSS150	W29
AK25	VSS71	VSS151	W28
AK22	VSS72	VSS152	W27
AK19	VSS73	VSS153	W26
AK16	VSS74	VSS154	U9
AK13	VSS75	VSS155	U8
AK10	VSS76	VSS156	U8
AK7	VSS77	VSS157	U6
AK4	VSS78	VSS158	U5
AJ25	VSS79	VSS159	U3
	VSS80	VSS160	U2

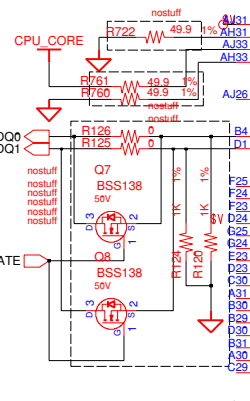
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T35	VSS161	VSS234	F22
T34	VSS162	VSS235	F19
T33	VSS163	VSS236	F30
T32	VSS164	VSS237	F27
T31	VSS165	VSS238	F22
T30	VSS166	VSS239	F21
T29	VSS167	VSS240	E18
T28	VSS168	VSS241	E15
T27	VSS169	VSS242	E10
T26	VSS170	VSS243	E9
T25	VSS171	VSS244	E8
T24	VSS172	VSS245	E8
T23	VSS173	VSS246	E7
T22	VSS174	VSS247	E6
T21	VSS175	VSS248	E5
T20	VSS176	VSS249	E4
T19	VSS177	VSS250	E3
T18	VSS178	VSS251	E1
T17	VSS179	VSS252	D35
T16	VSS180	VSS253	D32
T15	VSS181	VSS254	D28
T14	VSS182	VSS255	D25
T13	VSS183	VSS256	D20
T12	VSS184	VSS257	D17
T11	VSS185	VSS258	D13
T10	VSS186	VSS259	C34
T9	VSS187	VSS260	C29
T8	VSS188	VSS261	C27
T7	VSS189	VSS262	C25
T6	VSS190	VSS263	C25
T5	VSS191	VSS264	C25
T4	VSS192	VSS265	C10
T3	VSS193	VSS266	B22
T2	VSS194	VSS267	B19
T1	VSS195	VSS268	B17
	VSS196	VSS269	B13
	VSS197	VSS270	B13
	VSS198	VSS271	B13
	VSS199	VSS272	B11
	VSS200	VSS273	B9
	VSS201	VSS274	B7
	VSS202	VSS275	B5
	VSS203	VSS276	B3
	VSS204	VSS277	B3
	VSS205	VSS278	A35
	VSS206	VSS279	A32
	VSS207	VSS280	A29
	VSS208	VSS281	A26
	VSS209	VSS282	A26
	VSS210	VSS283	A26
	VSS211	VSS284	A3
	VSS212	VSS285	A3
	VSS213		
	VSS214		
	VSS215		
	VSS216		
	VSS217		
	VSS218		
	VSS219		
	VSS220		
	VSS221		
	VSS222		
	VSS223		
	VSS224		
	VSS225		
	VSS226		
	VSS227		
	VSS228		
	VSS229		
	VSS230		
	VSS231		
	VSS232		
	VSS233		

MEM1_VREF_DQ0

MEM1_VREF_DQ1

CHP3_DRAMRST_GATE



RESERVED

AK28	CFG0	RSVD28	L7
AK29	CFG1	RSVD29	AG7
AL26	CFG2	RSVD30	AE7
AL27	CFG3	RSVD31	AK2
AK26	CFG4	RSVD32	W9
AL29	CFG5		
AL30	CFG6		
AM31	CFG7	RSVD33	AT26
AM32	CFG8	RSVD34	AM33
AM30	CFG9	RSVD35	AJ27
AM28	CFG10		
AM26	CFG11		
AN28	CFG12		
AN31	CFG13		
AN26	CFG14		
AM27	CFG15	RSVD37	T8
AK31	CFG16	RSVD38	J16
AN29	CFG17	RSVD39	H16
		RSVD40	G16

RSVD28	L7
RSVD29	AG7
RSVD30	AE7
RSVD31	AK2
RSVD32	W9
RSVD33	AT26
RSVD34	AM33
RSVD35	AJ27
RSVD37	T8
RSVD38	J16
RSVD39	H16
RSVD40	G16

RSVD1	AR35
RSVD2	AT34
RSVD3	AT33
RSVD4	AP35
RSVD5	AR34
RSVD6	B34
RSVD7	A34
RSVD8	B35
RSVD9	C35
RSVD10	
RSVD11	
RSVD12	
RSVD13	AJ32
RSVD14	AK32
RSVD15	
RSVD16	
RSVD17	AH27
RSVD18	AN35
RSVD19	AM35
RSVD20	
RSVD21	AT2
RSVD22	AT1
RSVD23	AR1

RSVD41	B34
RSVD42	A34
RSVD43	B35
RSVD44	C35
RSVD45	
RSVD46	
RSVD47	
RSVD48	
RSVD49	
RSVD50	
RSVD51	AJ32
RSVD52	AK32
RSVD53	AH27
RSVD54	AN35
RSVD55	AM35
RSVD56	AT2
RSVD57	AT1
RSVD58	AR1

RSVD24	J20
RSVD25	B18
VCCIO_SEL_RSVD	A19
RSVD27	J15

FOR RPGA SOCKET
RSVD59 PIN SHOULD BE LEFT NC

KEY

B1

CFG Straps for Processor

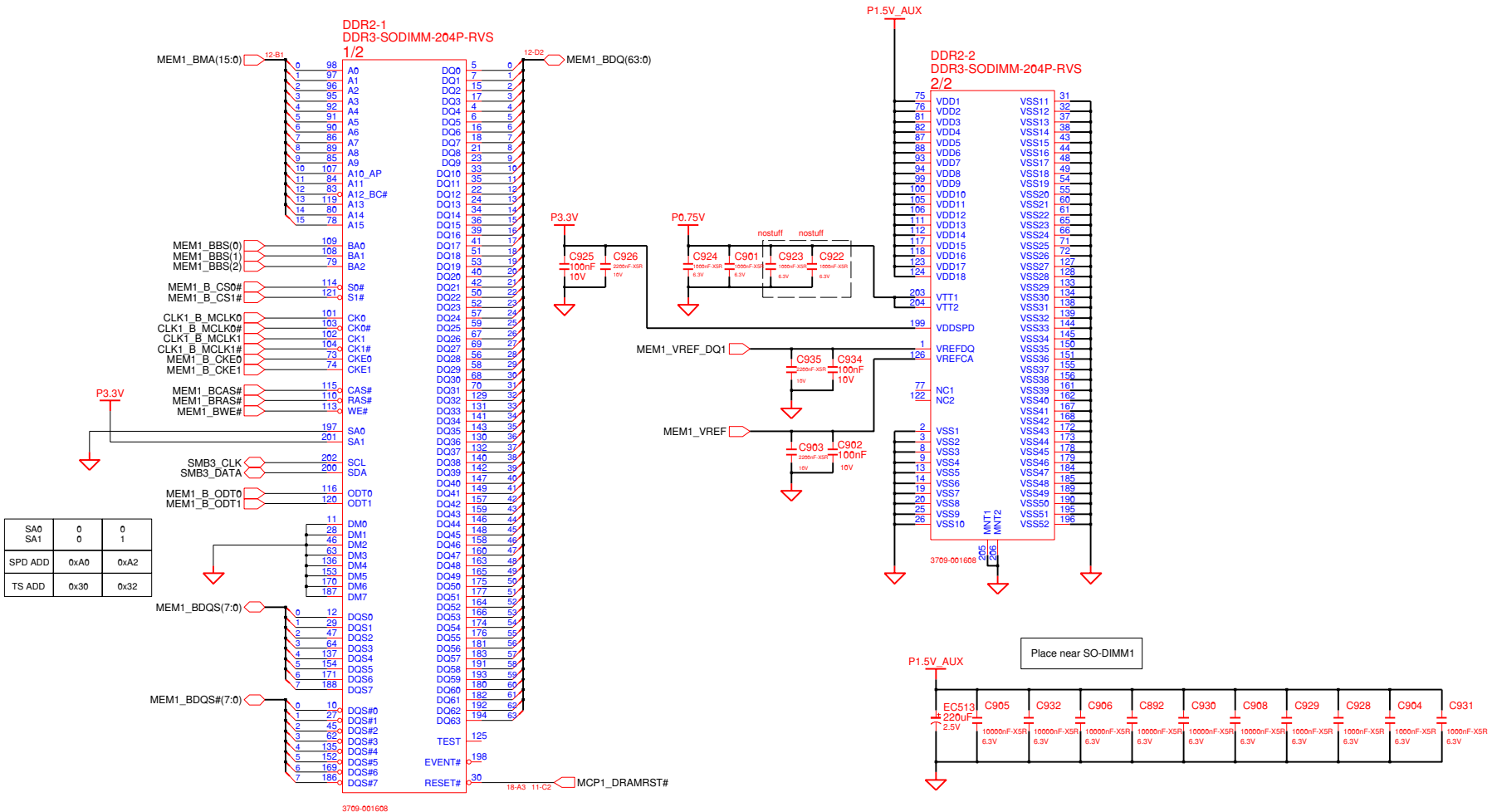
PEG STATIC LANE REVERSAL - CFG2 IS FOR THE 16X	
CFG2	1 : (DEFAULT) NORMAL OPERATION 0 : LANE REVERSED
PCIe PORT BIFURCACTION STRAPS	
CFG(6:5)	11 : (DEFAULT) X16 - DEVICE 1 FUNCTIONS 1 AND 2 DISABLED 10 : X8, X8 - DEVICE 1 FUNCTION 1 ENABLED ; FUNCTION 2 DISABLED 01 : RESERVED - (DEVICE 1 FUNCTION 1 DISABLED ; FUNCTION 2 ENABLED) 00 : X8, X4, X4 - DEVICE 1 FUNCTIONS 1 AND 2 ENABLED
Display Port Presence	
CFG4	1 : Disabled 0 : No DP device is connected to eDP - Enabled - (DP device is connected to eDP)
PEG DEFER TRAINING	
CFG7	1 : (DEFAULT) PEG TRAIN IMMEDIATELY FOLLOWING XPRESETB DEASSERTION 0 : PEG WAIT FOR BIOS FOR TRAINING

SO-DIMM#1 : 1st SO-DIMM

DDR SO-DIMM #1
Vinafix.com

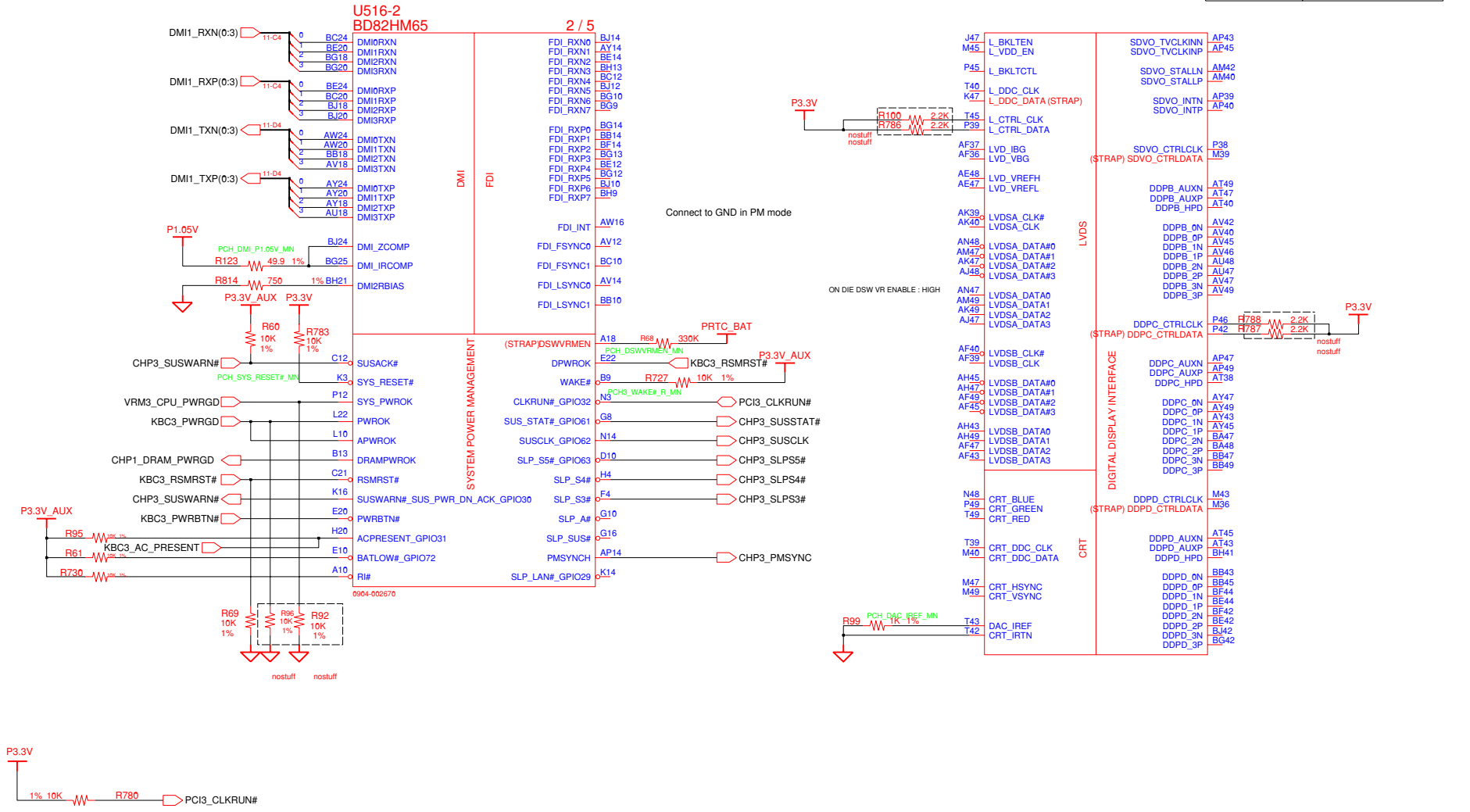
P/N : 3709-001608 (CONCRAFT)

P/N : 3709-001654 (Foxconn)

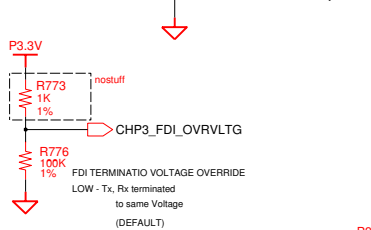
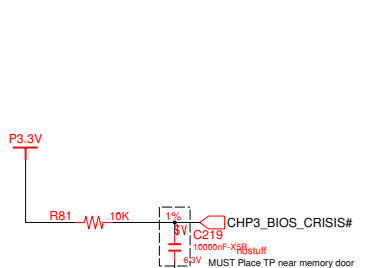
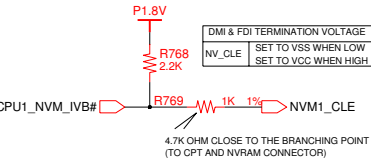


EX0: 33/27/48/24/14.318 MHz
EX2: 33/25/27/48/24/14.318 MHz
EX1.3: 27/48/14.318 MHz

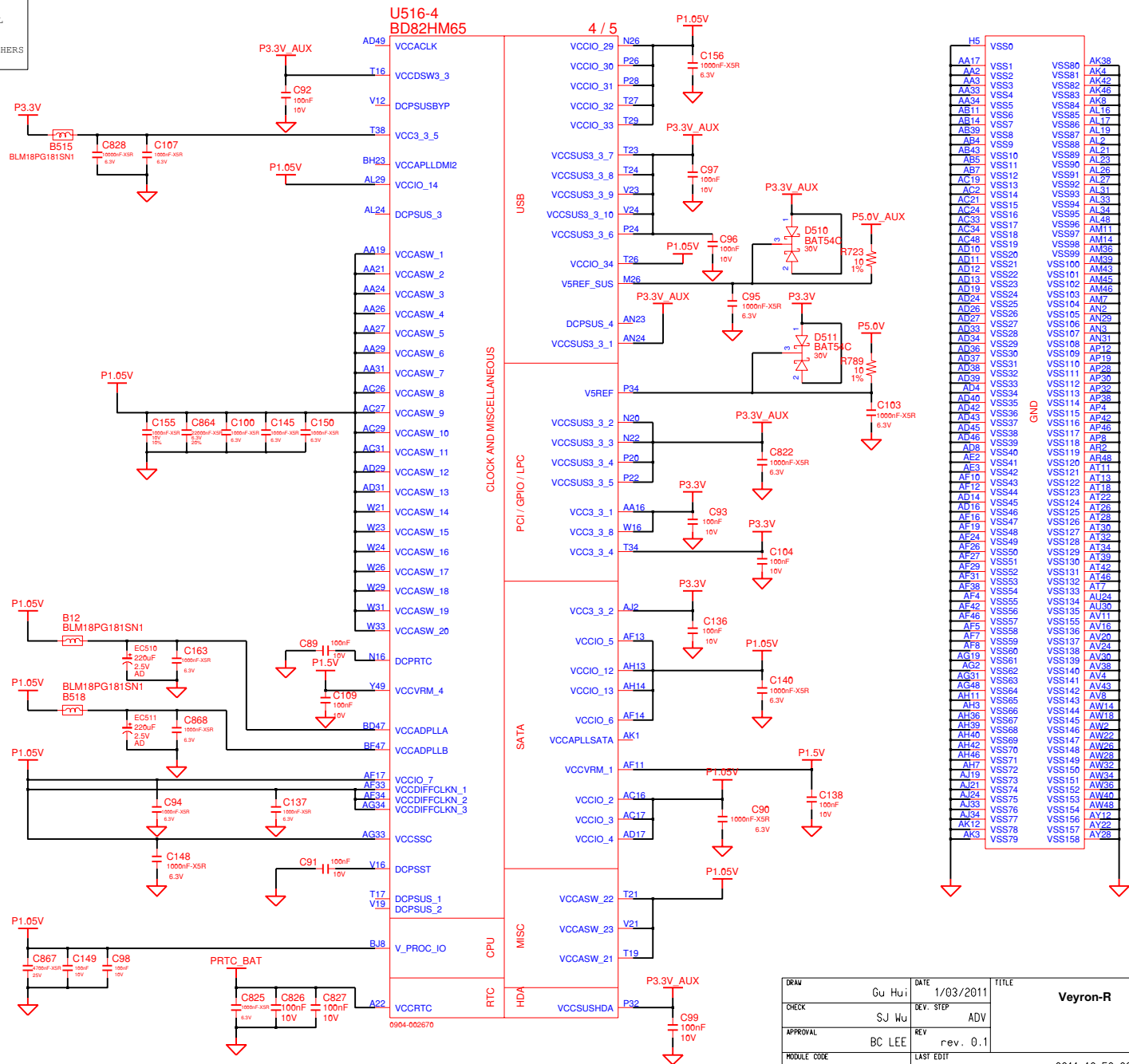
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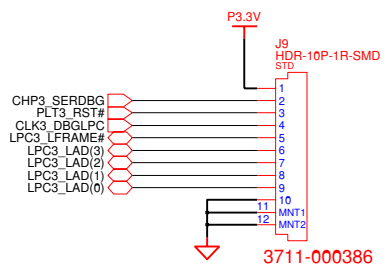
DDI PORT B DETECT	
SDVO_CTRL_DATA	1 PORT B DETECTED 0 PORT B NOT DETECTED



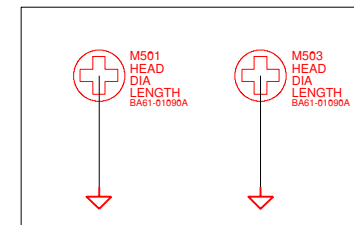
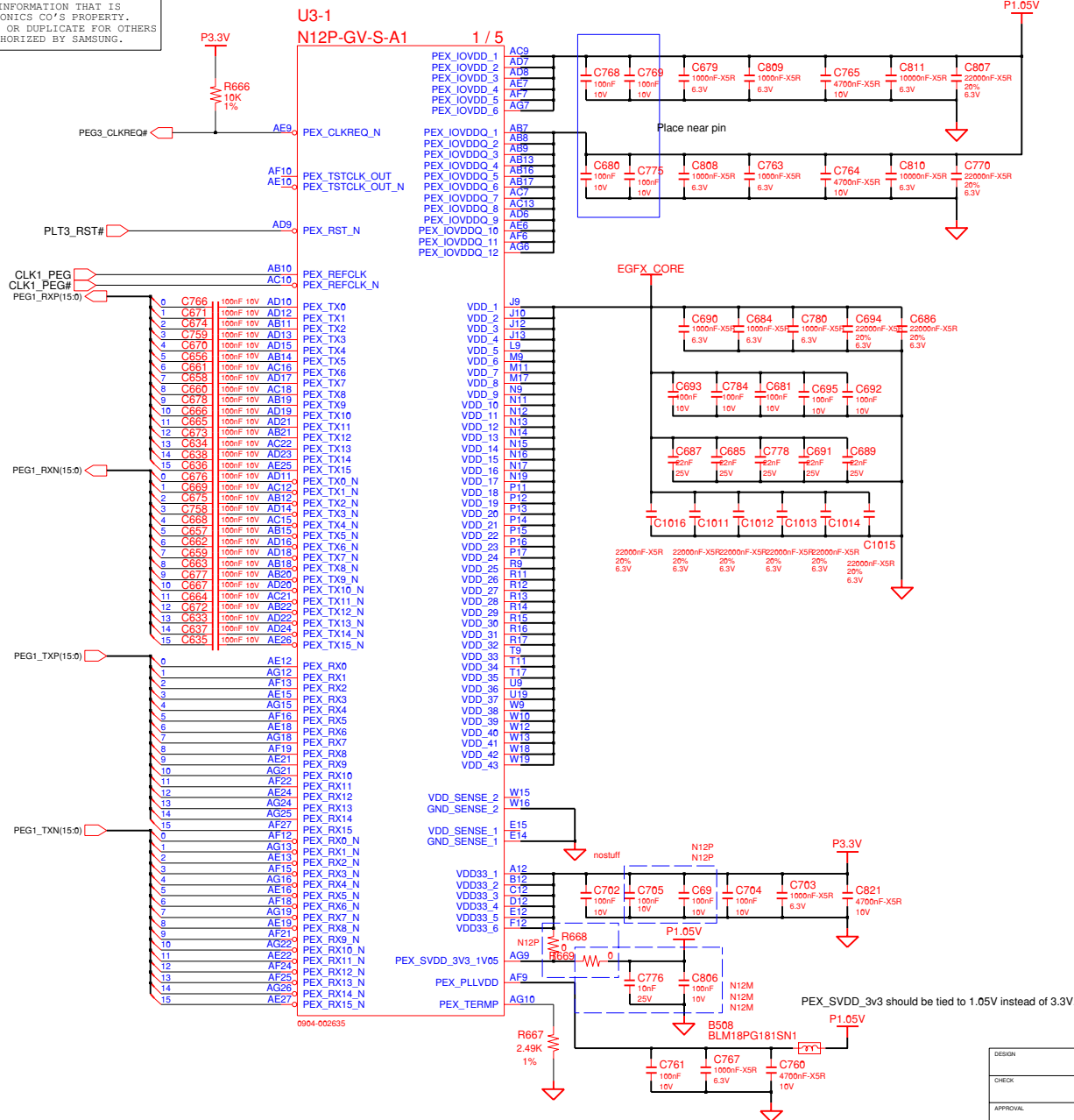
BOOT BIOS STRAP		
BBS_BIT	0	1
BBS_BIT0	0	1
BBS_BIT1	0	1
BBS_BIT2	0	1
BBS_BIT3	0	1
BBS_BIT4	0	1
BBS_BIT5	0	1
BBS_BIT6	0	1
BBS_BIT7	0	1
BBS_BIT8	0	1
BBS_BIT9	0	1
BBS_BIT10	0	1
BBS_BIT11	0	1
BBS_BIT12	0	1
BBS_BIT13	0	1
BBS_BIT14	0	1
BBS_BIT15	0	1
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BBS_BIT18	0	1
BBS_BIT19	0	1
BBS_BIT20	0	1
BBS_BIT21	0	1
BBS_BIT22	0	1
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BBS_BIT24	0	1
BBS_BIT25	0	1
BBS_BIT26	0	1
BBS_BIT27	0	1
BBS_BIT28	0	1
BBS_BIT29	0	1
BBS_BIT30	0	1
BBS_BIT31	0	1
BBS_BIT32	0	1
BBS_BIT33	0	1
BBS_BIT34	0	1
BBS_BIT35	0	1
BBS_BIT36	0	1
BBS_BIT37	0	1
BBS_BIT38	0	1
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BBS_BIT40	0	1
BBS_BIT41	0	1
BBS_BIT42	0	1
BBS_BIT43	0	1
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BBS_BIT45	0	1
BBS_BIT46	0	1
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BBS_BIT49	0	1
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BBS_BIT51	0	1
BBS_BIT52	0	1
BBS_BIT53	0	1
BBS_BIT54	0	1
BBS_BIT55	0	1
BBS_BIT56	0	1
BBS_BIT57	0	1
BBS_BIT58	0	1
BBS_BIT59	0	1
BBS_BIT60	0	1
BBS_BIT61	0	1
BBS_BIT62	0	1
BBS_BIT63	0	1
BBS_BIT64	0	1
BBS_BIT65	0	1
BBS_BIT66	0	1
BBS_BIT67	0	1
BBS_BIT68	0	1
BBS_BIT69	0	1
BBS_BIT70	0	1
BBS_BIT71	0	1
BBS_BIT72	0	1
BBS_BIT73	0	1
BBS_BIT74	0	1
BBS_BIT75	0	1
BBS_BIT76	0	1
BBS_BIT77	0	1
BBS_BIT78	0	1
BBS_BIT79	0	1
BBS_BIT80	0	1
BBS_BIT81	0	1
BBS_BIT82	0	1
BBS_BIT83	0	1
BBS_BIT84	0	1
BBS_BIT85	0	1
BBS_BIT86	0	1
BBS_BIT87	0	1
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80H PORT DEBUG

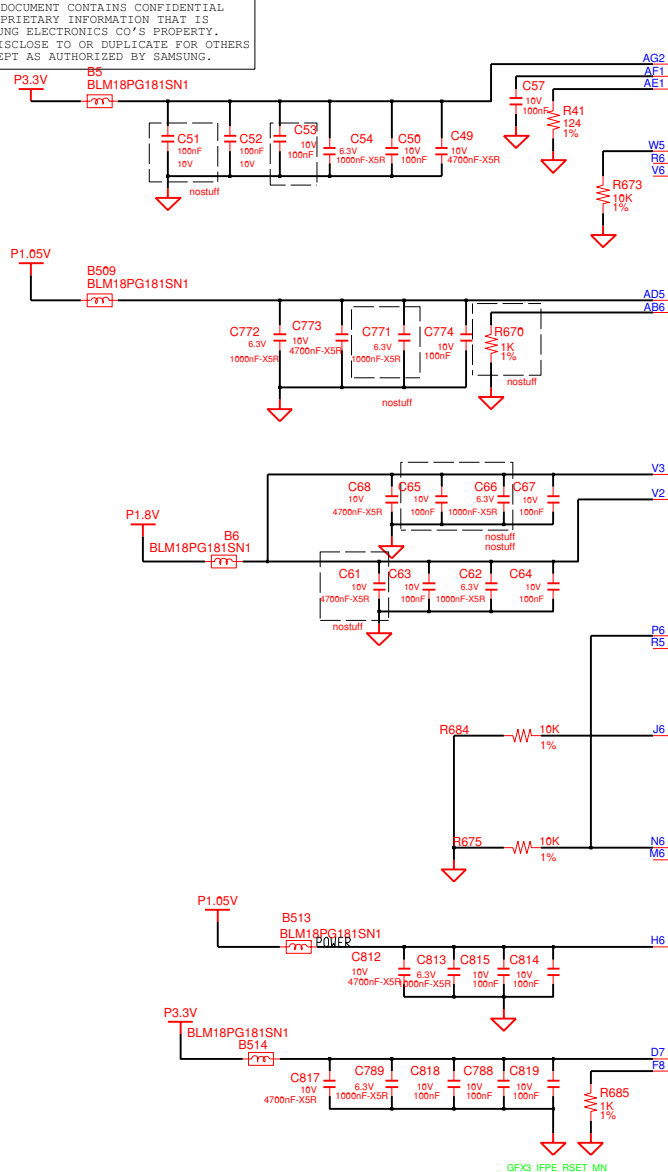


DESIGN	DATE	Veyron-R	SAMSUNG ELECTRONICS
CHECK	DEV. STEP		
APPROVAL	REV		
MODULE CODE	LAST EDIT		
		PAGE	OF



Graphic PEM

DESIGN	Gu Hui	DATE	1/03/2011	TITLE	Veyron-R	SAMSUNG
CHECK	SJ Wu	DEV. STEP	ADV		N12P_40NM(1/4)	ELECTRONICS
APPROVAL	BC LEE	REV	rev. 0.1		N12P_40NM(1/4)	PART NO.
MODULE CODE		LAST EDIT				BA41-01XXXX
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U3-3 N12P-GV-S-A1

3 / 5

AG2
AF1
AE1

DACA_VDD
DACA_VREF
DACA_RSET

DACB_VDD
DACB_VREF
DACB_RSET

IFPA_TXD0_N
IFPA_TXD0

IFPA_TXD1_N
IFPA_TXD1

IFPA_TXD2_N
IFPA_TXD2

IFPA_TXD3_N
IFPA_TXD3

IFPB_TXD4_N
IFPB_TXD4

IFPB_TXD5_N
IFPB_TXD5

IFPB_TXD6_N
IFPB_TXD6

IFPB_TXD7_N
IFPB_TXD7

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IFPE_L0_N
IFPE_L0

GPIO15

GPIO19

GPIO0

GPIO1

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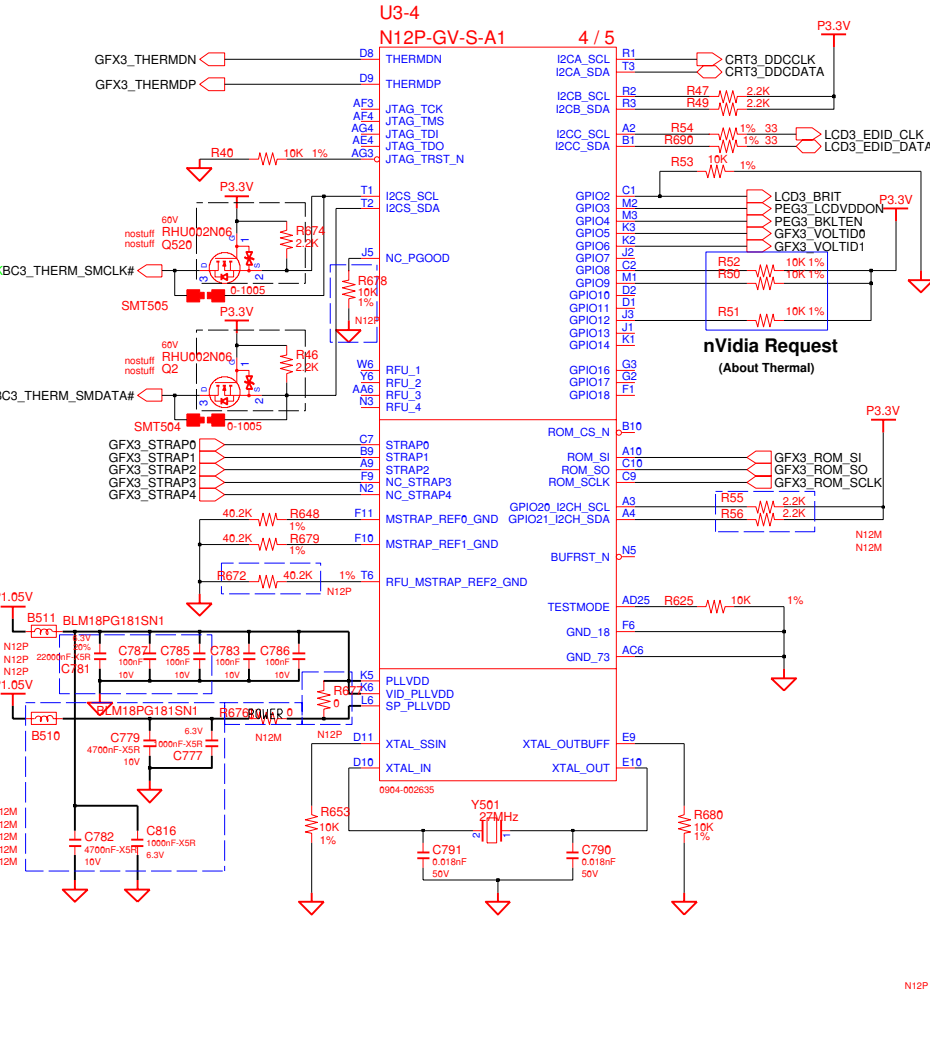
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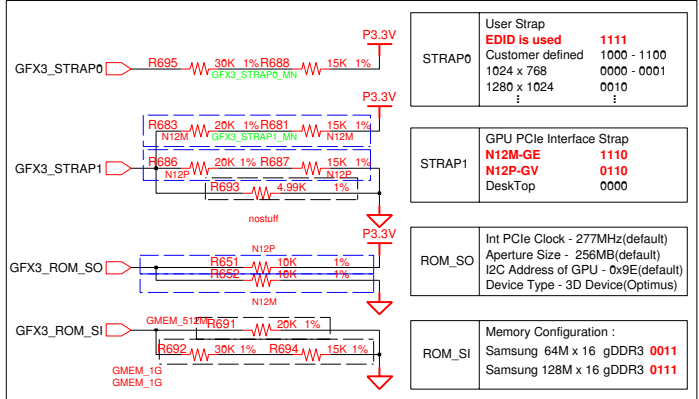
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GPIO285

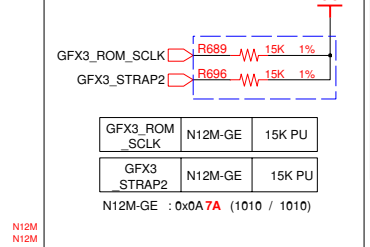
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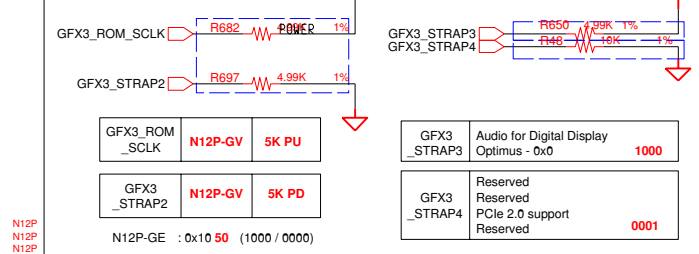
Function Straps



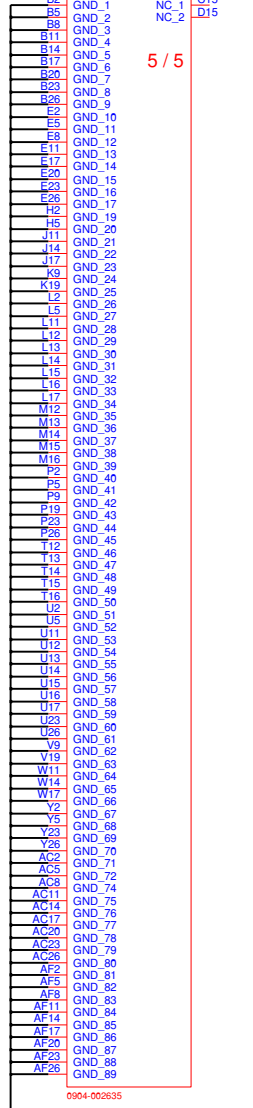
Chip Select Straps (N12M-GB1)



Chip Select Straps (N12P-GV)



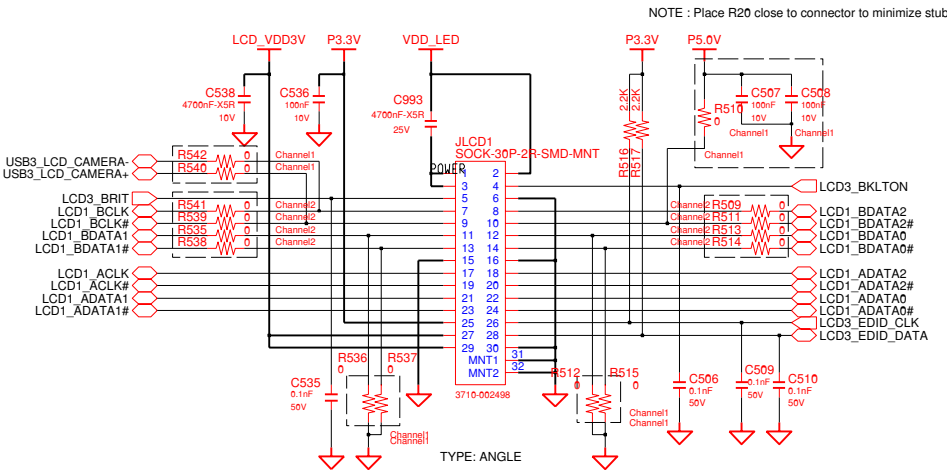
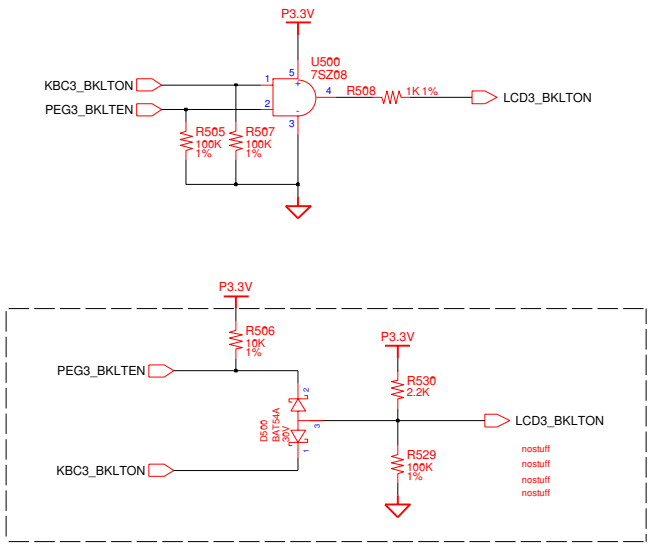
U3-5 N12P-GV-S-A1



LVDS LOGIC

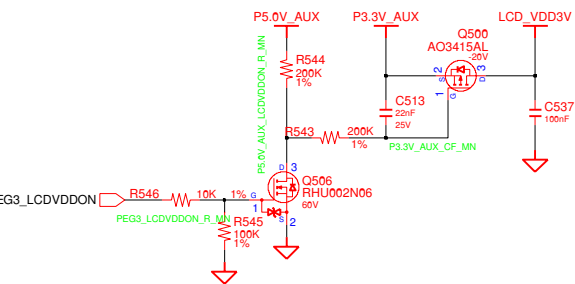
1Ch. LCD Connector + CAMERA

Backlight On

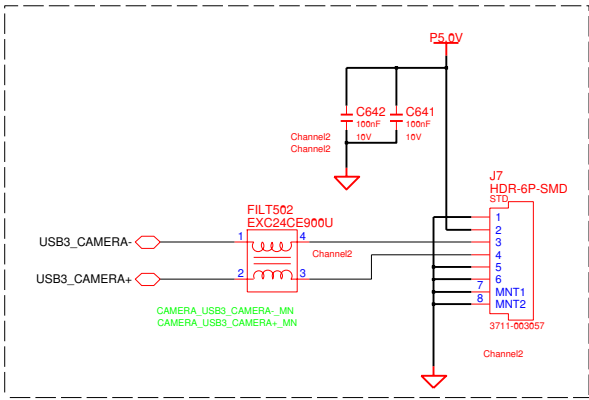
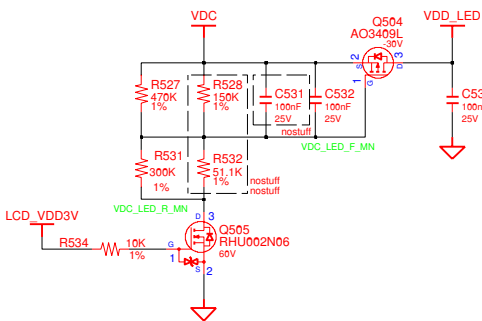


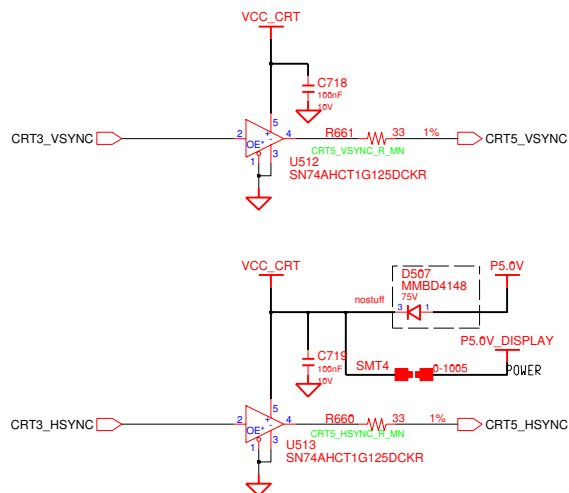
CAMERA CONN FOR 2ch LVDS

LCD Power



LED Power

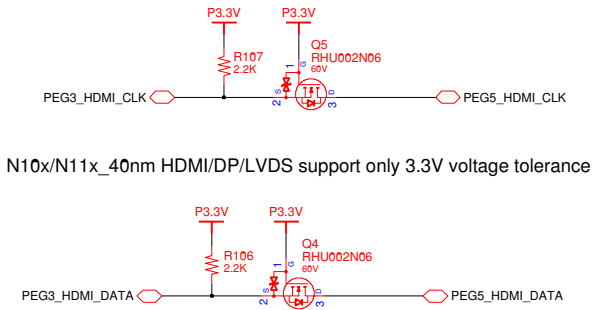




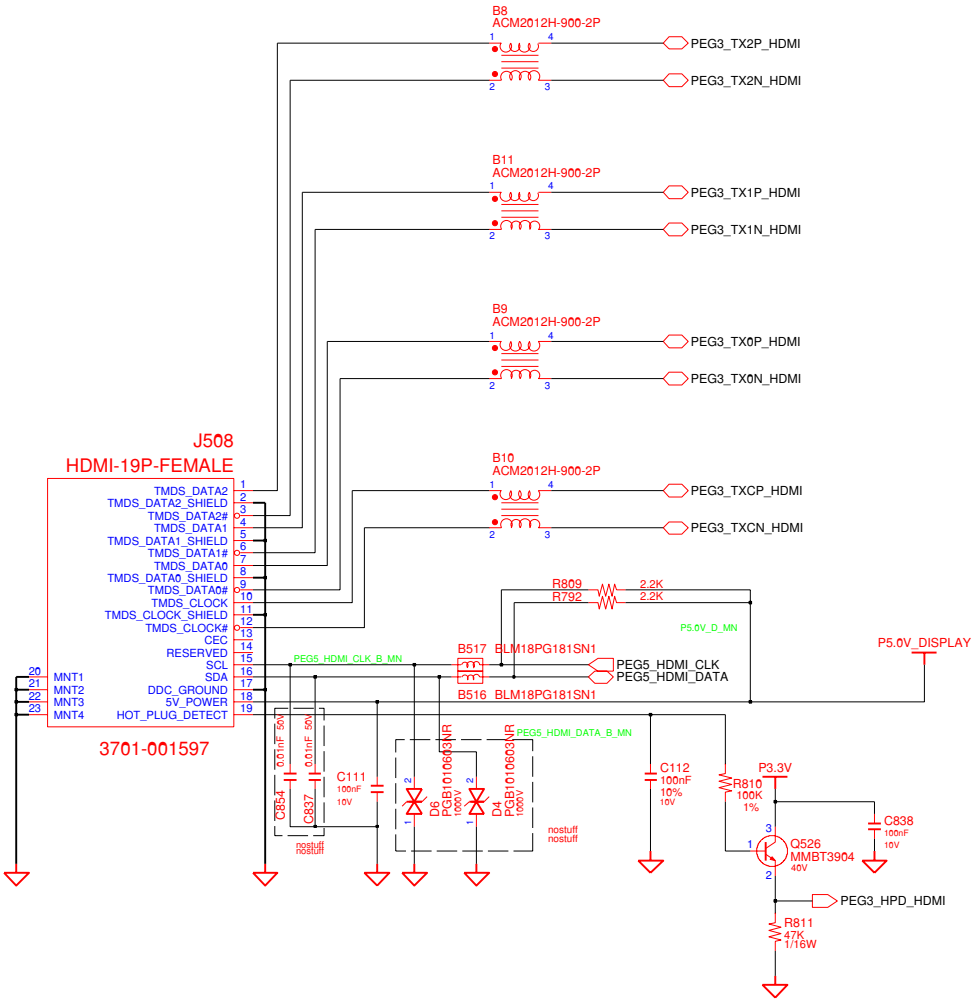
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CHECK	SJ Wu	DEV. STEP	ADV		
APPROVAL	BC LEE	REV	rev. 0.1		
MODULE CODE	LAST EDIT				
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HDMI Graphic

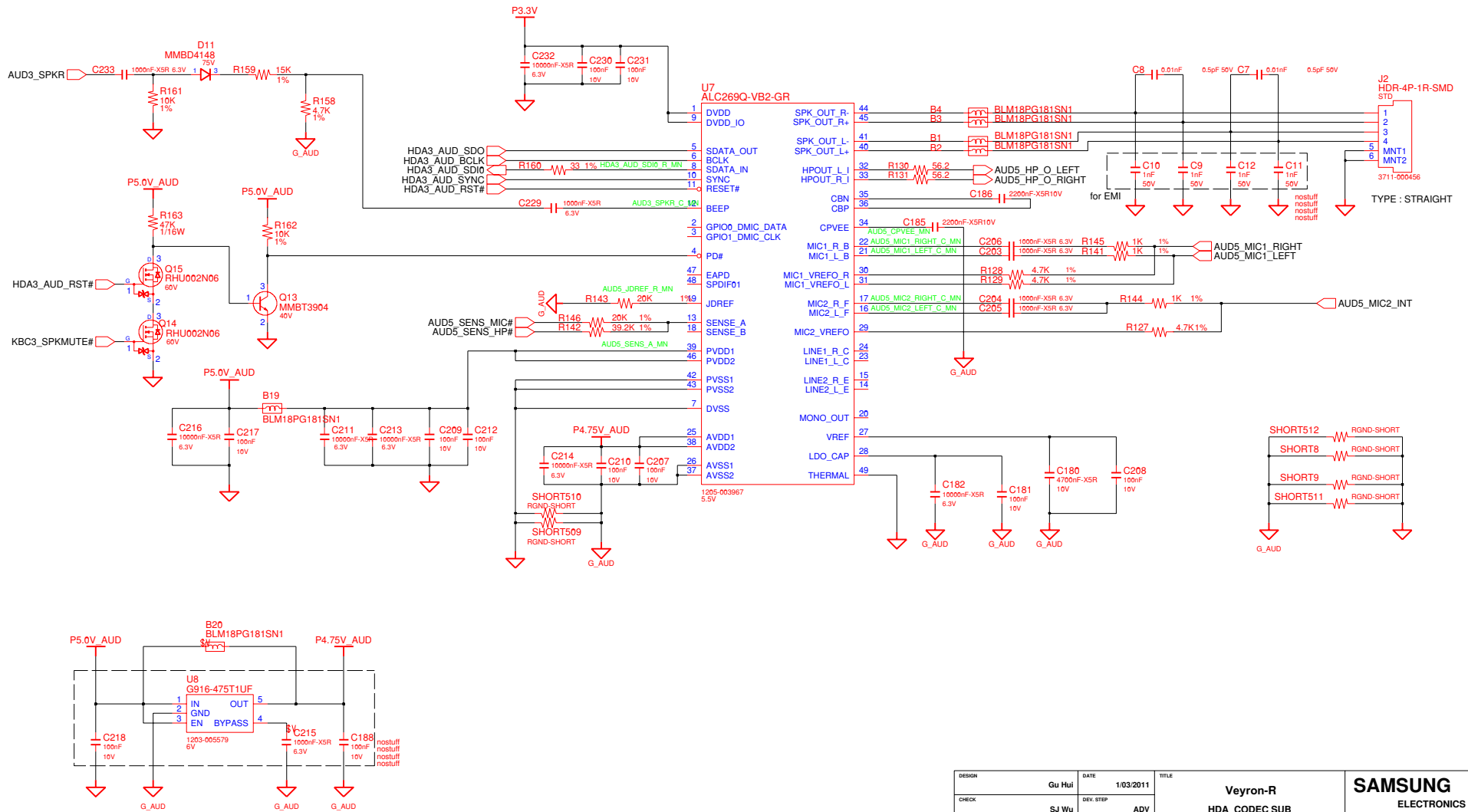
FOR HDMI VERIFICATION TEST



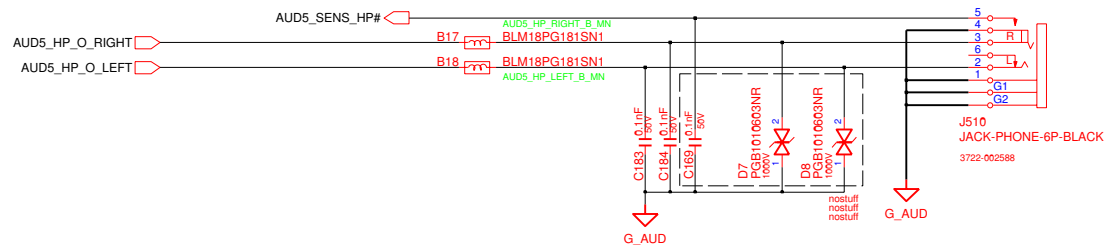
N10x/N11x_40nm HDMI/DP/LVDS support only 3.3V voltage tolerance



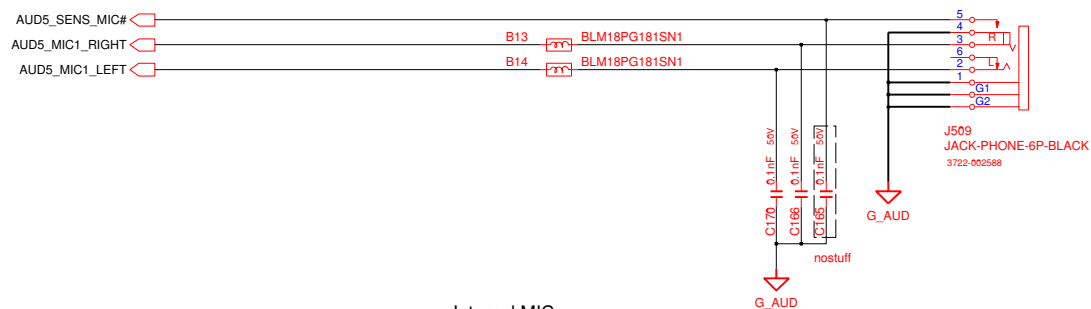
HD AUDIO



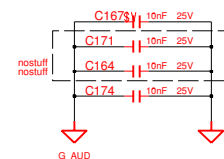
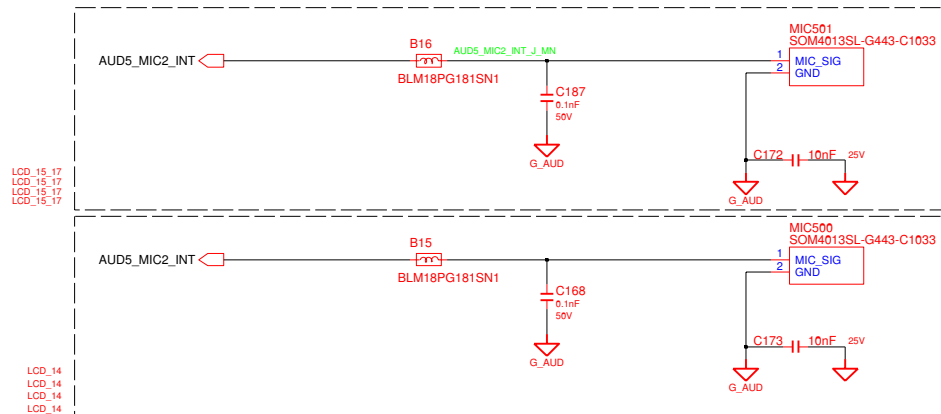
HEADPHONE



MIC JACK

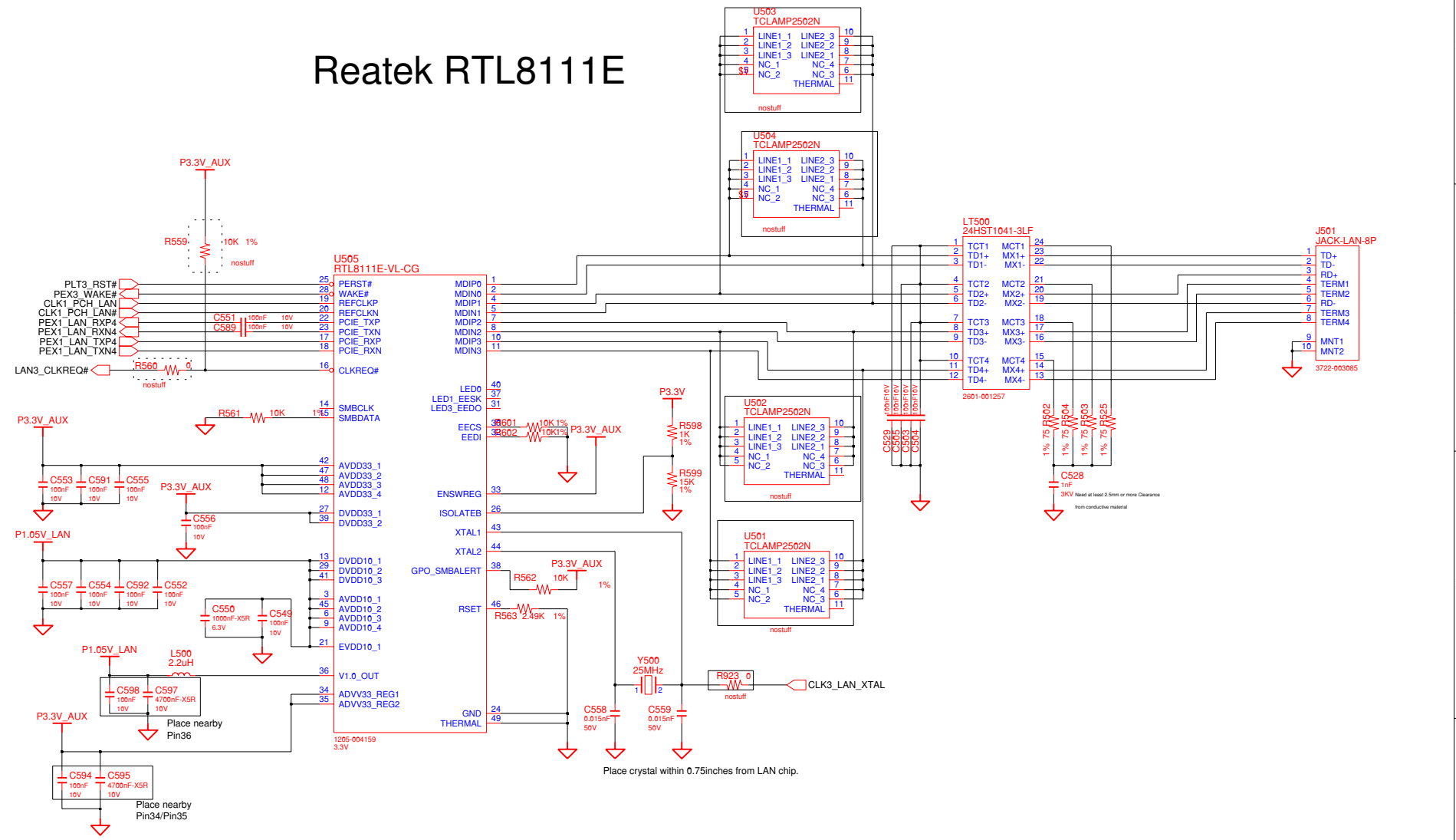


Internal MIC

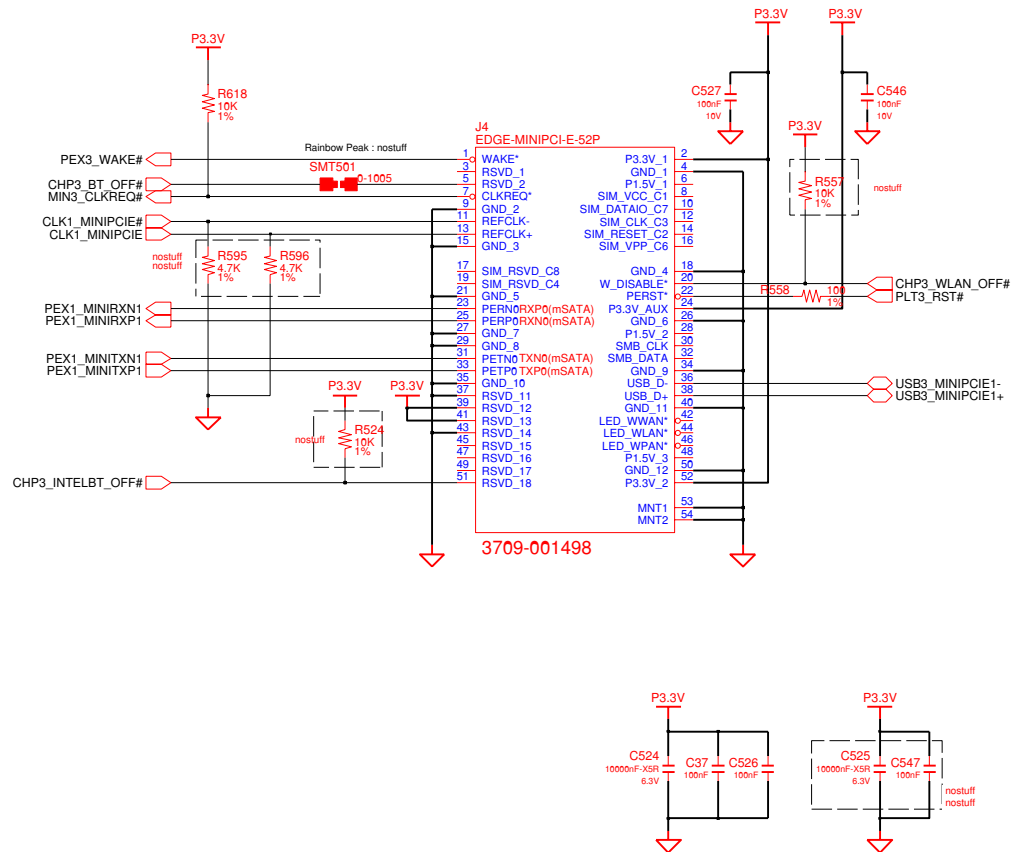


DESIGN	Gu Hui	DATE	1/03/2011	TITLE Veyron-R HDA_CODEC & LED SUB AUDIO JACK & LED SUB	SAMSUNG ELECTRONICS
CHECK	SJ Wu	DEV. STEP	ADV		
APPROVAL	BC LEE	REV	rev. 0.1		
MODULE CODE	LAST EDIT				
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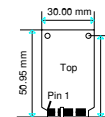
Reatek RTL8111E



WLAN, 4mm



Mini PCI Express Card

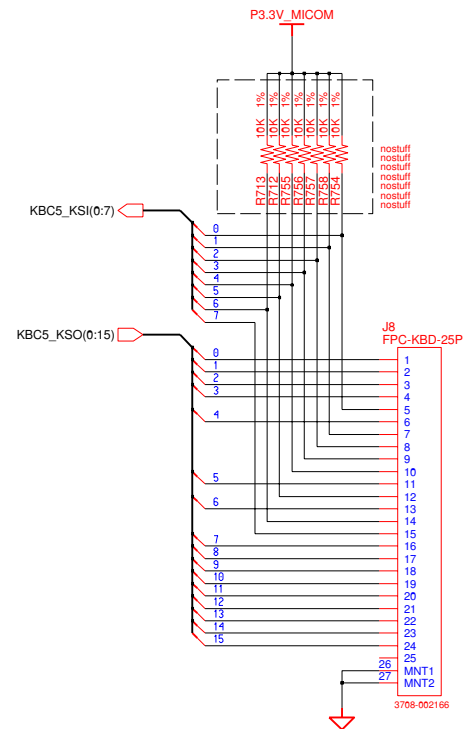


Odd Pins : Top side
Even Pins : Bottom Side

DESIGN	Gu Hui	DATE	1/03/2011	TITLE	Veyron-R MINI_PCIE_CONN WLAN	SAMSUNG ELECTRONICS	
CHECK	SJ Wu	DEV. STEP	ADV				PART NO. BA41-01XXXX
APPROVAL	BC LEE	REV	rev. 0.1				
MODULE CODE		LAST EDIT	January 20, 2011 18:59:20 PM				
				PAGE	31	OF	48

Micom Glue Logic

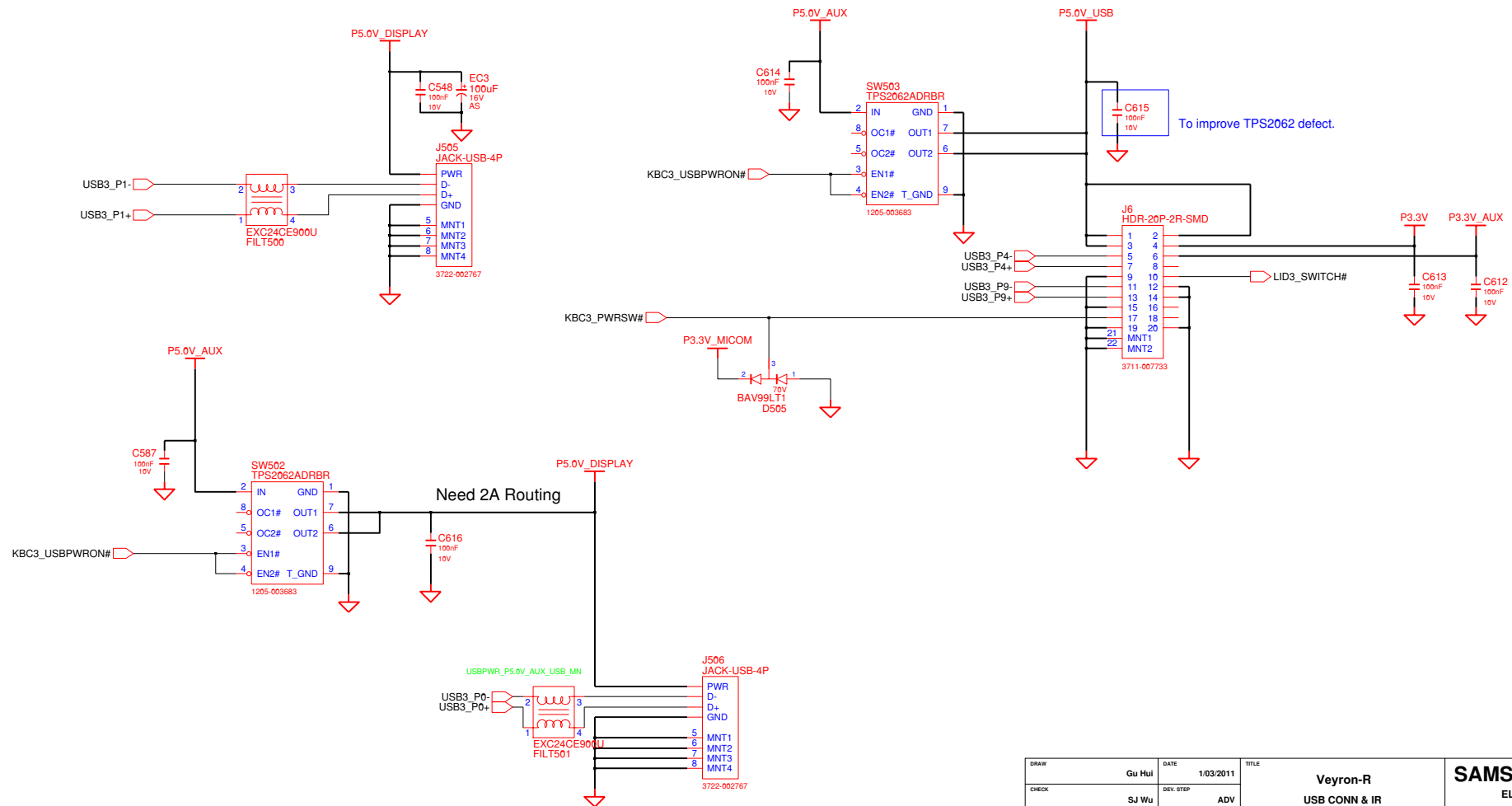
KEYBOARD



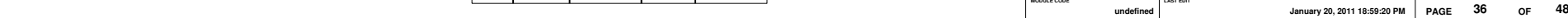
DRAW	Gu Hui	DATE	1/03/2011	TITLE	Veyron-R	SAMSUNG
CHECK	SJ Wu	DEV. STEP	ADV	MICOM GLUE LOGIC	MICOM GLUE LOGIC	ELECTRONICS
APPROVAL	BC LEE	REV	rev. 0.1	MICOM GLUE LOGIC	PART NO.	BA41-01XXXA
MODULE CODE	LAST EDIT			January 20, 2011 18:59:20 PM	PAGE	34 OF 48

POWER S/W SUB B'D CONNECTOR

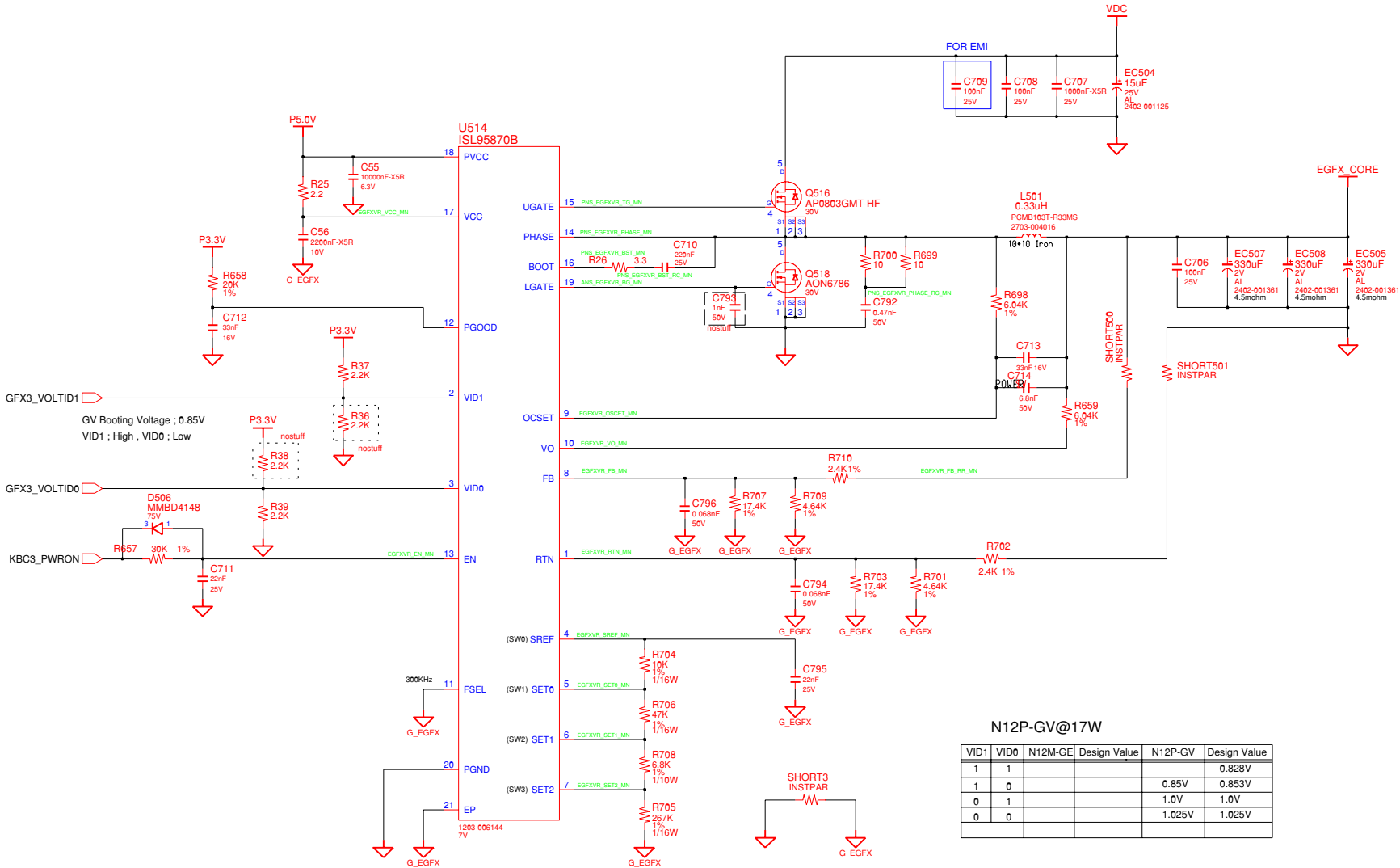
MAIN to SUB



DRAW	Gu Hui	DATE	1/03/2011	Veyron-R USB CONN & IR USB & IR	SAMSUNG ELECTRONICS	
CHECK	SJ Wu	DEV. STEP	ADV			
APPROVAL	BC LEE	REV	rev. 0.1			
PART NO.			BA41-01XXXXA			
MODULE CODE	LAST EDIT				January 20, 2011 18:59:20 PM	PAGE 35 OF 48



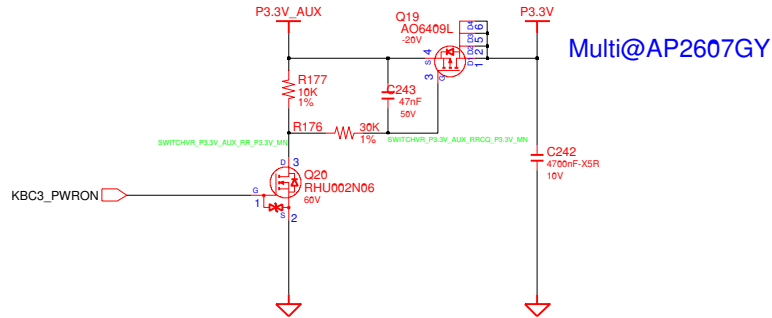
External GFX Core Power



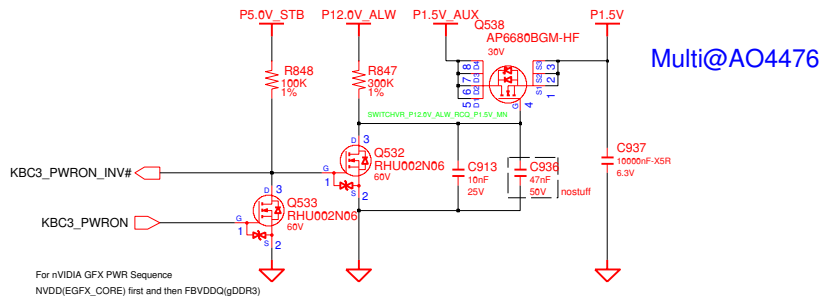
Switched Power

P5.0V -> P3.3V -> EGFX_CORE -> P1.8V ->P1.5V -> P0.75V -> P1.05V -> P0.8V_VCCSA -> CPU_CORE

Switched Power On (P3.3V)



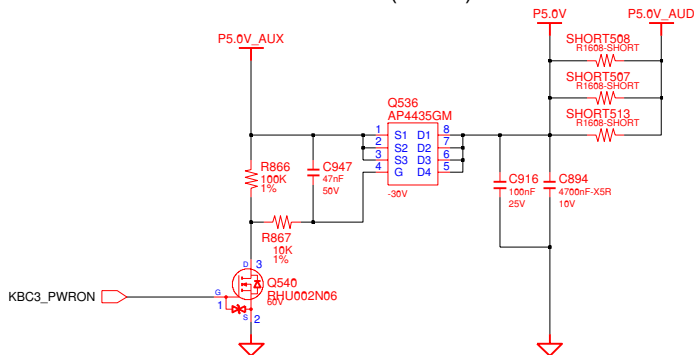
Switched Power On (P1.5V)



For nVIDIA GFX PWR Sequence
NVDD(EGFX_CORE) first and then FBVDDQ(gDDR3)

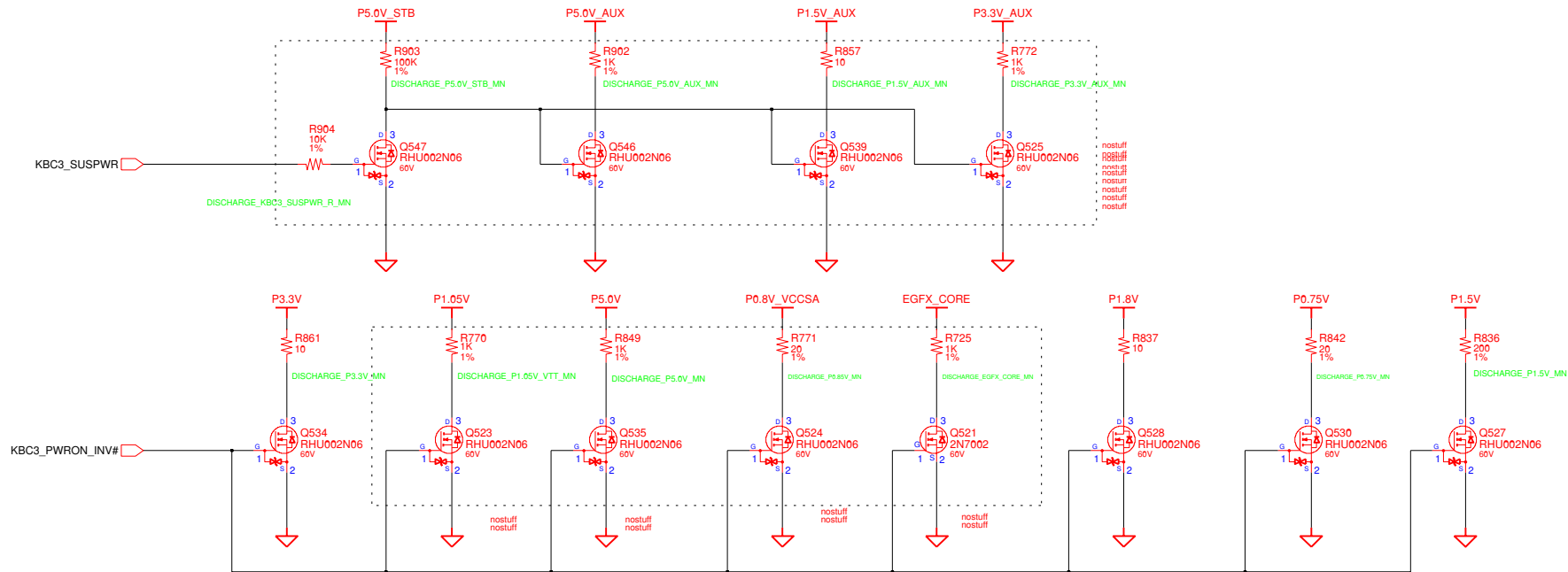
Switched Power On (P5.0V)

Multi@Si4435DDY



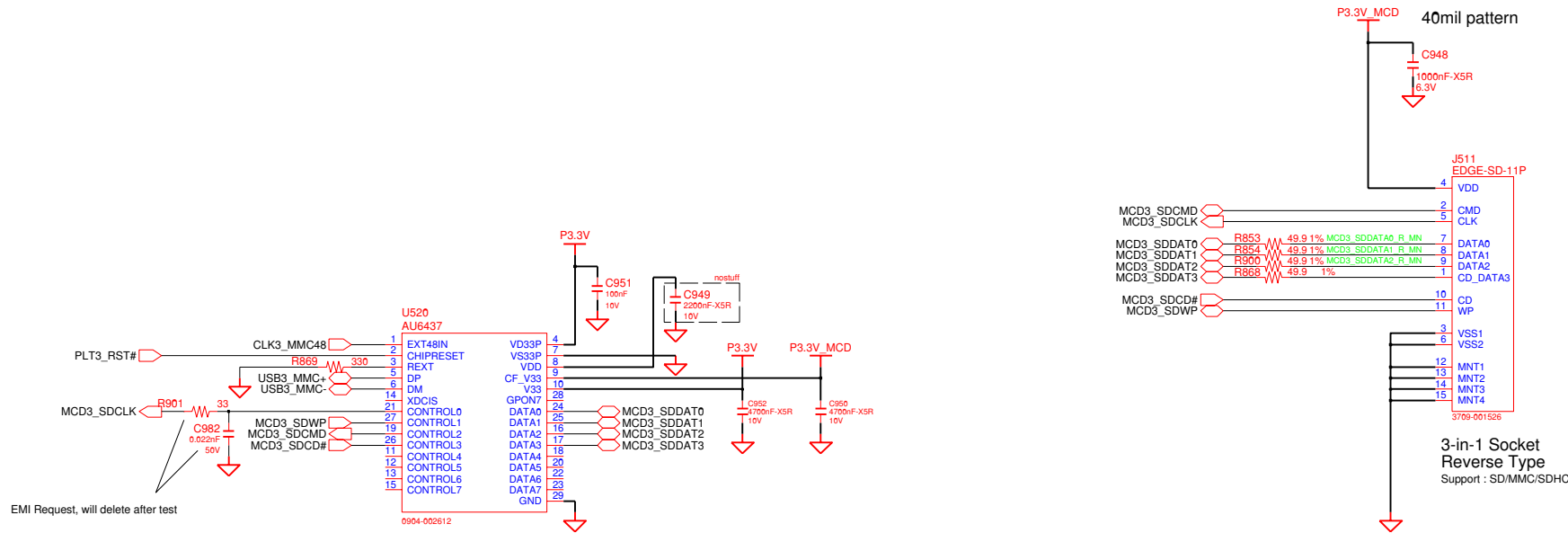
DRAW	Gu Hui	DATE	1/03/2011	TITLE	Veyron-R	SAMSUNG
CHECK	SJ Wu	DEV. STEP	ADV	PWR_MV_DISCHARGER	ELECTRONICS	
APPROVAL	BC LEE	REV	rev. 0.1	SWITCHED POWER	PART NO.	BA41-01XXXX
MODULE CODE	undefined	LAST EDIT	January 20, 2011 18:58:20 PM	PAGE	43	OF 48

POWER DISCHARGER

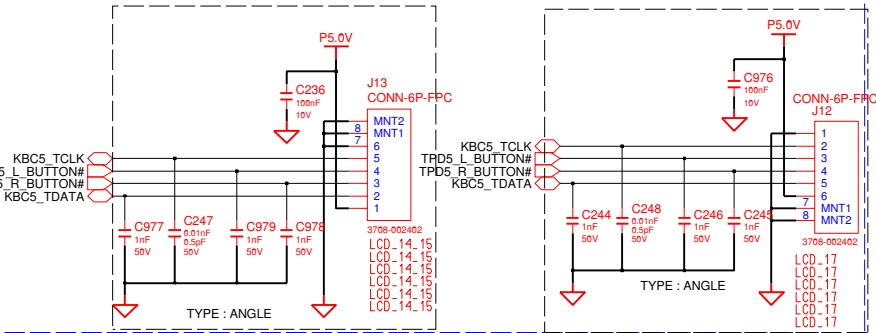


DESIGN	Gu Hui	DATE	1/03/2011	TITLE	Veyron-R SUB BOARD1 Power Discharger	SAMSUNG ELECTRONICS PART NO. BA41-01XXXXA
CHECK	SJ Wu	DEV. STEP	ADV			
APPROVAL	BC LEE	REV	rev. 0.1			
MODULE CODE		LAST EDIT				
January 20, 2011 18:58:20 PM						PAGE 45 OF 48

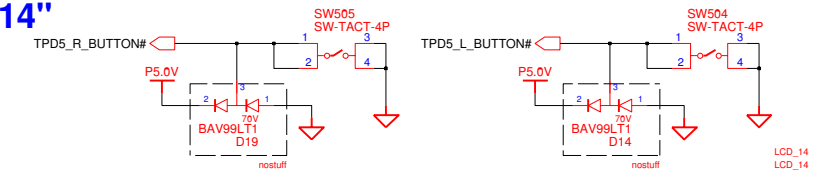
AU6437 (4-in-1)



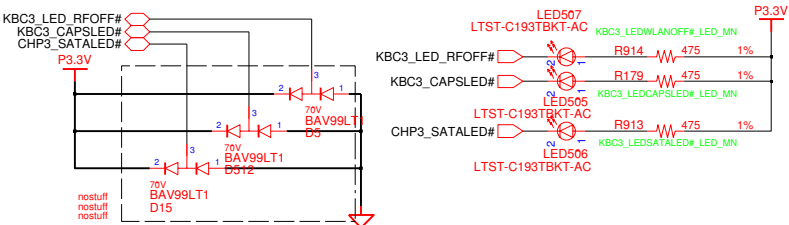
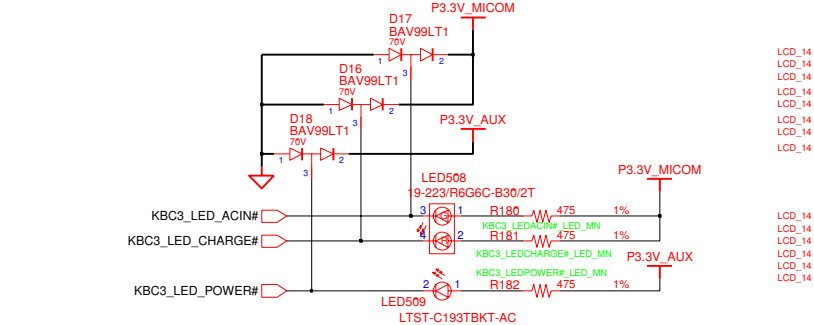
TOUCHPAD



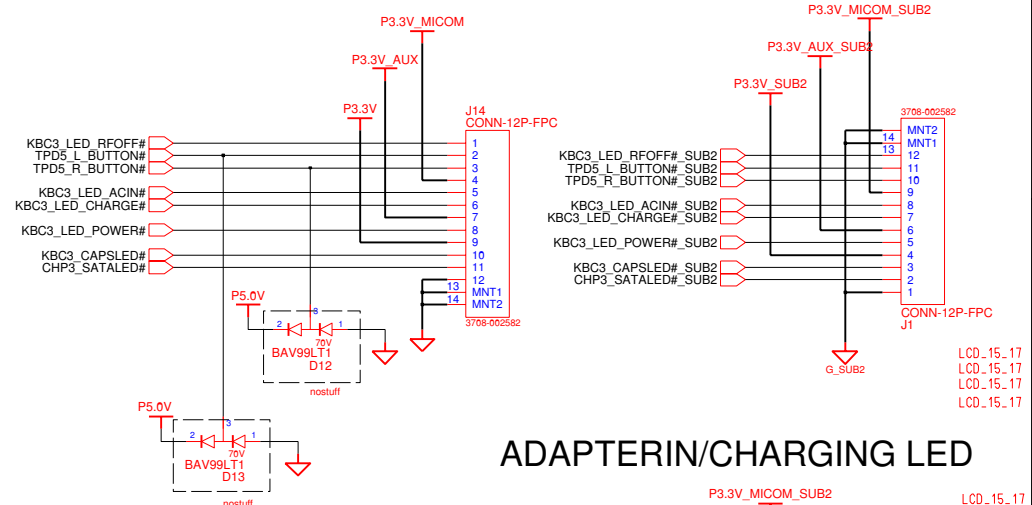
14"



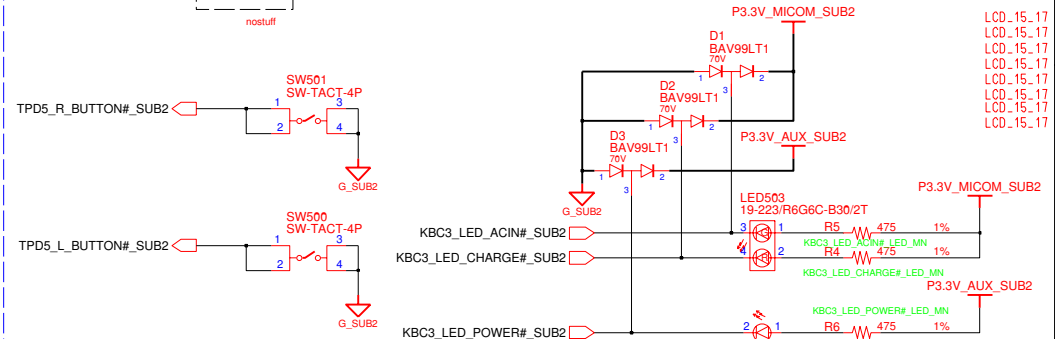
ADAPTERIN/CHARGING LED



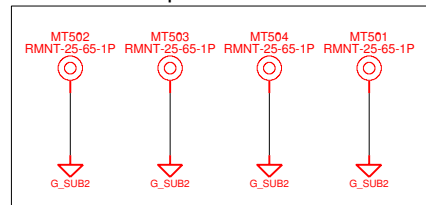
15.6" & 17.3" TOUCHPAD MAIN TO SUB TOUCHPAD SUB TO MAIN



ADAPTERIN/CHARGING LED



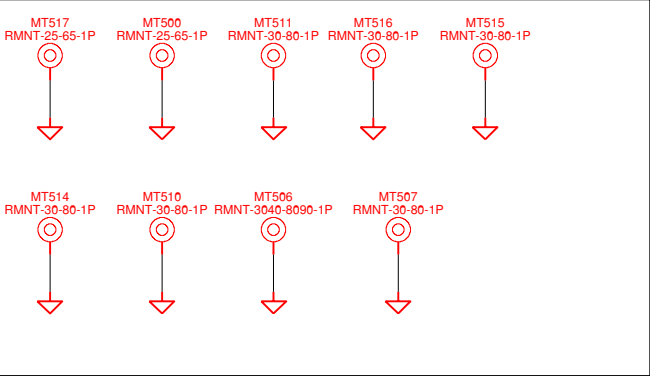
Touchpad Mount Hole



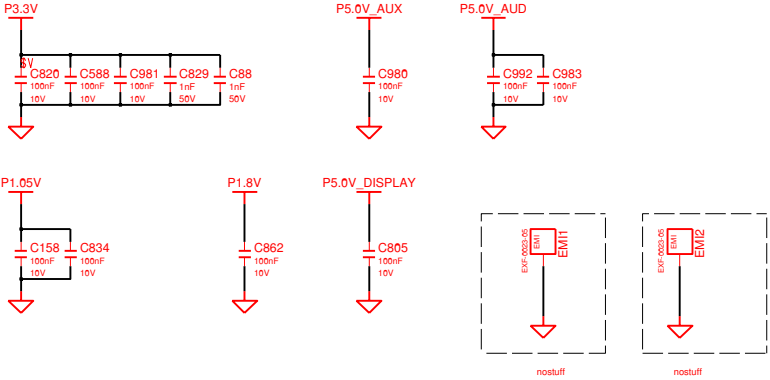
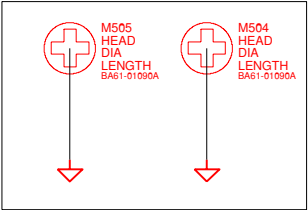
DRAW	MS YANG	DATE	1/03/2011	TITLE	Veyron-R
CHECK	MK KIM	DEV. STEP	ADV		Touchpad
APPROVAL	BL LEE	REV	rev. 0.3		Touchpad
MODULE CODE		LAST EDIT			

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Mainboard Mount ((25-65)X2EA, (30-80)X7EA)



PCH Thermal



DESIGN	MS YANG	DATE	1/03/2011	TITLE	Veyron-R MNT hole MNT hole	SAMSUNG ELECTRONICS
CHECK	MK KIM	DEV. STEP	ADV			
APPROVAL	BL LEE	REV	rev. 0.3			
MODULE CODE				LAST EDIT		PART NO.
				January 18, 2011 08:10:20 AM		BA41-01XXXXA
				PAGE	48	OF 48